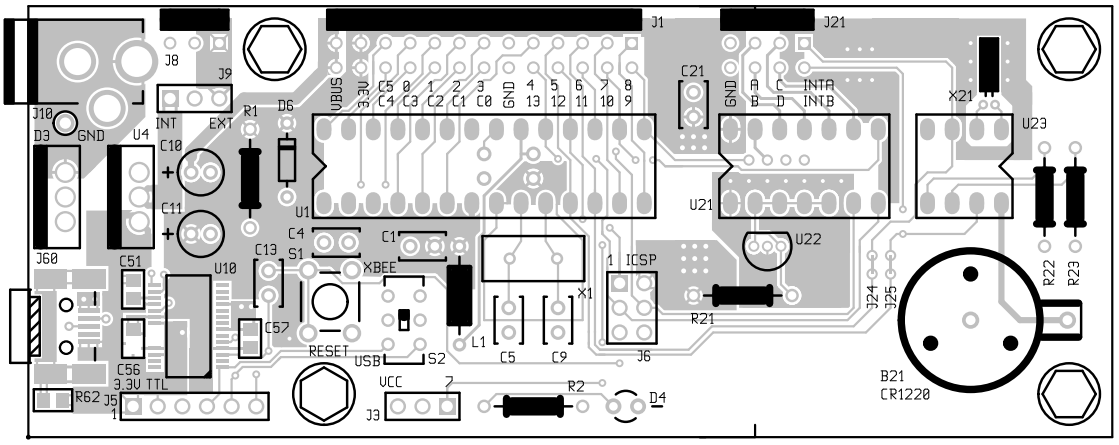

NB1A Description

The NB1A is a microcontroller development system that is compatible with the Arduino software environment. For system development a variety of peripherals are available.

Features

- Replaceable and upgradeable CPU
- Compatible with the Arduino development tools.
- ATmega328 running at 12MHz with a V_{CC} of 3.3V.
- 4.4" x 1.75"
- Atmega I/O connections are wired to a single 26 pin header. DAC and RTC interrupt output lines are wired to an 8 pin header. Application boards can be mounted parallel using vertical connectors, co-planar using right-angle connectors or remotely using a cable.
- DAC Features
  - Four channels, eight bits per channel.
  - Reference – 1.24V, ±0.5% (initial accuracy), 50ppm per °C typical drift, 140ppm per °C max drift,
  - SPI Interface
- RTC Features
  - Real-Time Clock (RTC) counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Valid Up to 2100
  - Two Time-of-Day Alarms
  - Programmable Square-Wave Output
  - Powered by a CR1220 coin cell.
  - I^2C Serial Interface
- The board can be built with either a USB interface or with a six pin header for use with an USB to serial cable. The USB interface circuitry includes transient suppression.
- ICSP port (3.3V levels)
- A/D reference supply filtered per Atmel specification.
- Reset circuit per Atmel specification.
- Power supply is jumpered between either an LDO or an external 3.3V supply. The LDO input is diode or'ed from a wall adapter or the USB 5V supply.
- Compatible with the ZB1 accessories which include an LCD interface board and a prototyping board.

1 ECOs – NB1A Rev1 PCB

There are two known fabrication mistakes on the NB1A Rev1 PCB. These are minor mistakes that affect the assembly of the board not the functionality. *Perform these reworks prior to starting the assembly procedure*

- The diameter of the drill holes for the watch crystal (`X21`) are ≈3mils too small. Although some combinations of crystal leads and PCB holes will have sufficient clearance for assembly most will not. The hole has been re-drilled to a diameter of 16mils. You should top and bottom solder the leads since the hole may no longer be plated through.
- The connection from `R21` to the V_{CC} copper plane is missing (left side of the resistor). To connect `R21` to the V_{CC} copper plane scrape the solder mask with an X-acto knife, bend the `R21` lead and solder. You will need a fair amount of flux since the plane has a large thermal mass.

2 ZB1 Accessories

The NB1A cannot be connected directly to a ZB1-PB1 prototyping board or the ZB1-LCD-CHAR interface with right-angle connectors. `J21` on the NB1A interferes with circuitry on both of these peripherals. If `J21` is not populated or is changed to a vertical connector there is no issue. The boards can be connected with wire or in a backplane without issue.

3 Assembling the NB1A

Semiconductors are electrostatic-sensitive devices. Proper ESD handling precautions need to be taken to avoid damage.

The Bill of Materials (BOM) and Component List are in section 10. For full page assembly drawings see Figure 1 (top) and Figure 2 (bottom).

Extra care needs to be taken when soldering the right-angle connector(s) – `J1`, `J21`, `J8` (opt) and `J4` (opt). The outer edge of the connector bodies should not protrude over the edge of the board. After soldering and the connector pins should be parallel to the board.

A DC source with current limiting is useful for testing each section of the NB1A as you build it.

All of the headers supplied with the kit are breakaway headers. The single row headers, `J3` (3x1), `J5` (6x1), `J9` (3x1) may come as individual headers or as strips that need to be broken. Most kits will contain either two 6x1 headers or one 12x1. Break this headers to create `J3`, `J5` and `J9`.

If you are not building the USB circuit proceed to subsection 3.2.

3.1 USB Circuit Assembly

Solder the top side components:

- U10 - FT232RL
- C57, C56, C51
- R62
- J60

Solder the bottom side components:

- U55
- R59
- R58

At this point clean the flux off of the top and bottom side of the board. After the board is cleaned visually inspect the board for solder shorts, opens and cold solder joints. If possible power up `U10` with a current limited +3.3V supply by attaching clip leads to the pads of the LDO (`U4`). +3.3V connected to `U4` pin 2 and GND connects to `U1` pin 1. The current drawn from the +3.3V supply should not exceed a few milliamperes. If it does then check for solder bridges on `U10` and `U55`.

3.2 Bottom Side Components

- F1
- C2, C3

3.3 Power Supply Circuit Assembly

Solder the top side components:

- C10, C11

  C10 and C11 are polarized parts. The long lead is the positive. The short lead is the negative. Make sure that the **positive** *lead is inserted into positive hole in the PCB*

- U4

  Be careful to not mixup U4 and D3. U4 is marked `MC33269T-3.3G` *Make sure that the tab is aligned to the tab marking on the PCB.*

- D3

  Be careful to not mixup D3 and U4. D3 is marked `MBR1545CTG` *Make sure that the tab is aligned to the tab marking on the PCB.*

- J9
- J10

- J8 (optional)

  J8 enables the usage of an external 3.3V power source with the NB1A. If you do not need this function then you can omit the installation of J8. J8 is not included in the kit.

At this point clean the flux off of the top and bottom side of the board. After the board is cleaned visually inspect the board for solder shorts, opens and cold solder joints.

3.3.1 Testing the Power Supply Circuit

If possible apply power through `J10` with a current limited +5V supply. The current drawn from the +5V supply should not exceed a few milliamperes. If it does then verify the orientation on `C10`, `C11`, `D3`, `U4`.

3.4 Microcontroller Circuit Assembly

Solder the top side components:

- R1

  The tolerance of R1 is not critical. Some kits include a 5% resistor others include a 1% resistor. The 5% resistor has four color bands (brown, black, orange, gold). The 1% resistor has five color bands (brown, black, black, red, brown)

- D1

  Line the cathode marking on D1 with the cathode marking on the silkscreen

- C13, C1, C4 (optional).

  C4 is optional and is not included in the kit. It is meant for applications that require additional filtering of the reset line. Applications that use USB download or ISP programmers like the AVRISPMKII will not require additional filtering. Also, the reset function that uses the /RTS line from the USB interface will not function with C4 installed.

- L1

  The value of inductor L1 is not critical. Kits will contain an inductor with a value between 10µH and 15µH

- D4

  The negative lead of the LED is the short lead. Align the short lead with the negative marking on the PCB.

- R2

  The tolerance of R2 is not critical. Some kits include a 5% resistor others include a 1% resistor. The 5% resistor has four color bands (red, red, brown, gold). The 1% resistor has five color bands (red, red, brown, black, brown).

- J3

- X1, C5, C9

- U1 (socket)

- J6

- J1, J21

  The J1 and J21 that are included with the NB1A Kit are right angle connectors. If your application requires parallel board mounting or a cable connection then replace J1 and J21 with vertical headers. A 2x13 receptacle can also be used.

- J4 (optional).

At this point clean the flux off of the top and bottom side of the board. After the board is cleaned visually inspect the board for solder shorts, opens and cold solder joints. After inserting an ATmega328 into the `U1` socket the microcontroller section of the NB1A should be fully functional. If possibly apply power through `J10` with a current limited +5V supply. The current drawn should not exceed 10mA (20mA if the `J3` jumper is installed in the VCC position).

3.5 RTC Circuit Assembly

`R22` and `R23` are the I^2C pullups. The value included the NB1A kit is 4.7KΩ. If you are running the I^2C bus at lower frequencies you could increase the value of these resistors. If your application has external pullups you should remove these resistors (See subsection 8.1).

The DS1337 interrupt lines, `/INTA` and `/INTB` are jumpered to PD6 (Arduino pin 6) and PD5 (Arduino pin 5) respectively. To disconnect `/INTA` cut jumper J24. To disconnect `/INTB` cut jumper J25 (See subsection 8.2).

- R22, R23

  The tolerance of R22 and R23 is not critical. Some kits include a 5% resistor others include a 1% resistor. The 5% resistor has four color bands (yellow, violet, red, gold). The 1% resistor has five color bands (yellow, violet, black, brown, brown).

- B21 battery holder

- X21 crystal

  If you are assembling a revision one PCB then see section 1.

- U23 socket

3.6 DAC Circuit Assembly

NB: *If you are assembling a revision one PCB you need to perform an ECO prior to assembling the DAC section. See section 1.*

The DAC latch pin, `LDAC`, is connected to PB1 (Arduino pin 9). The `LDAC` pin enables all of the outputs to be updated at the same time. If your application does require simultaneous update of all channels then `LDAC` can be grounded. To ground `LDAC` cut jumper `J22` and connect the the `U21` side of `J22` to `J23` (either side).

- R21
- U22
- C21
- U21 socket

3.7 Electro-mechanical Components

The electro-mechanical components are sensitive to washing. Place all of these last and lightly wash afterward. If water does get into these components let them dry out before applying power.
Solder the top side components:

- S2
- S1

3.8 Mounting Hardware

Space has been provided for four #2 hex standoffs and washers.

3.9 IC Installation and Test

Remove each IC from the antistatic foam and insert it into the appropriate socket aligning the notch in the IC package with notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

- ATmega328 (`U1`)
- TLV5620 (`U21`)
- DS1337 (`U32`)

The board is now ready to program. To test the programming using the Arduino tools (see section 6).

4 IO Connectors

J1	13x2 header	I/O connections from the ATmega328. See Table 2
J5	6x1 header	USB header for an FTDI TTL-232R-3V3 cable. This is only installed if the USB circuit is not populated.
J6	3x2 header	ICSP header
J8	3x1 header	External 3.3V regulated voltage input.
J9	3x1 jumper	Jumper to switch between the external 3.3V input and the on board LDO.
J10	2.1mm Power Jack	5V to 15V unregulated DC. The power dissipation in U4 needs to be kept below one watt.
J21	4x2 header	I/O connections for the real-time clock and the DAC. See Table 3
J60	USB Mini-B	

Table 1: NB1A connectors

4.1 J1 Header

ATmega328 Pins (Arduino Pins)		J1 Pin		ATmega328 Pins (Arduino Pins)	
PB0 (**8**)	14	1	2	PB1 (**9**)	15
PD7/AIN1 (**7**)	13	3	4	PB2 (**10**)	16
PD6/AIN0 (**6**)	12	5	6	PB3/MOSI (**11**)	17
PD5 (**5**)	11	7	8	PB4/MISO (**12**)	18
PD4 (**4**)	6	9	10	PB5/SCK (**13**)	19
GND		11	12	GND	
PD3 (**3**)	5	13	14	PC0/ADC0 (**A0**)	23
PD2 (**2**)	4	15	16	PC1/ADC1 (**A1**)	24
PD1 (**1**)		17	18	PC2/ADC2 (**A2**)	25
PD0 (**0**)		19	20	PC3/ADC3 (**A3**)	26
PC5/ADC5/SCL (**A5**)	28	21	22	PC4/ADC4/SDA (**A4**)	27
+3.3V		23	24	+3.3V	
VBUS		25	26	VBUS	

Table 2: J1 Pinout

5 Electrical Hints

5.1 Power Supply

The NB1A can be powered by a wall adapter, the USB port or an external regulated 3.3V supply. The wall adapter and the USB port are diode or'ed and are connected to the input of a LDO regulator (U4). Jumper J9 selects between the two power sources – INT is the LDO regulator (U4), EXT is the power source connected to J8.

Power Jumper in the Internal Position

Power Jumper in the External Position

It is critcal to keep the power dissipation in the LDO regulator (U4), to less than one watt. The voltage drop across U4 is

$$V_{drop} = V_{in} - 0.5V$$

where V_{in} is the greater of the wall adapter voltage or +5V (USB 5V supply). The power dissipated in U4 is given by

$$P_{diss} = V_{drop} \cdot I_{system}$$

where I_{system} is the load of the NB1A plus its peripheral circuitry.

5.2 Powering from the USB Port

The intial startup load of a device connected to the USB port must not exceed 10μF in parallel with 44Ω ((USB-IF, 2000a)). Peripheral circuitry attached to the NB1A may produce a system load that exceeds the specification.

5.3 V_{BUS}

V_{BUS} is the unregulated voltage at the cathode of the or'ing diode (D3). Applications that require current beyond the current rating of the LDO regulator (U4) should use V_{BUS}. Since the only volage drop between the input power source and V_{BUS} is the V_f of the or'ing diode (D3) it is more efficient to use V_{BUS} rather than the +3.3V supply as an input voltage for other power conversions.

5.4 Debug LED

The debug LED, `D4`, can be connected to the +3.3V supply or to `U1` pin 13 (PD7) of the ATmega328. `U1` pin 13 corresponds to Arduino pin "7".

LED jumper in the VCC position

LED jumper in the Pin 7 position

6 Application Hints

6.1 Downloading a program to the NB1A

1. Place switch S2 in the USB position.
2. The NB1A is ready for download. It may be necessary to press the reset button prior to starting the download.

6.2 Downloading a bootloader

The NB1A is powered from 3.3V. Any device that connects to the NB1A needs to output 3.3V TTL levels. The Atmel `AVRATAVRISPMKII` and Ladyada USBtiny are compatible with the NB1A.

To use the Ladyada USBtiny remove the USBtiny jumper, JP3, and plug the USBtiny cable into the NB1A ICSP header. With JP3 removed the USBtiny output buffer (IC2) is powered by the V_{cc} from the NB1A (3.3V). The USBtiny output buffer (IC2) is a `74AHC125` which will tolerate 5V levels when powered from a 3.3V supply.

7 Programming the NB1A

The NB1A can be programmed using the Arduino tools (version `0011` or more recent). Kits contain an ATmega328. From the `Tools->Board` menu select the `Arduino Deicimila w/ ATmega328`.

To download a program the UART switch S2 must be in the USB position.

The NB1A uses a 12MHz XTAL. The Arduino tools are setup for boards with a 16MHz XTAL. If you do not change the tool setup you will need to adjust the baud rate of the serial port. For example – to get a baudrate of 9600 it is necessary to run the command:

```
Serial.begin(12800)
```

This baudrate setting value comes from the following equation:

$$\text{baud rate setting} = \frac{16\text{MHz}}{12\text{MHz}} \cdot 9600$$

Description		J22 Pin
/INTA	DS1337 /INTA (U23)	1
/INTB	DS1337 /INTB (U23)	2
C	TLV5620 DACC (U21)	3
D	TLV5620 DACD (U21)	4
A	TLV5620 DACA (U21)	5
B	TLV5620 DACB (U21)	6
GND		7
GND		8

Table 3: J22 Pinout

8 Real-Time Clock

The NB1A real-time clock (RTC) consists of a DS1337 that is powered by a CR1220 coin cell. Communication to the DS1337 is through the I^2C interface (a.k.a. two-wire or TWI). The I^2C pullup resistors are on board (4.7KΩ). The interrupt lines, `/INTA` and `/INTB` are jumpered to PD6 (Arduino pin 6) and PD5 (Arduino pin 5) respectively. There are no pullup resistors on the interrupt lines. If external pullups are not added then the internal pullups of the ATmega328 need to be used.

Programming the RTC requires a software library for the DS1337 and for the TWI interface. Both of these libraries are on the wiblocks site.

8.1 I^2C Pullup Resistors

The maximum bus capacitance of the I^2C bus is 400pF. Unless a large number of devices are on the bus or devices are connected using long cables an NB1A system will not get close to this limit. The DS1337 represents a maximum load of 10pF.

The mimunum pullup resistance is 966Ω ($\frac{V_{CC}-0.4V}{3mA}$). The maximum value pullup resistance is

$$R_{pullup(max)} = \begin{cases} \frac{1000nS}{C_{BUS}} & \text{if } F_{SCL} <= 100kHz, \\ \frac{300nS}{C_{BUS}} & \text{if } 100kHz < F_{SCL} <= 400kHz. \end{cases}$$

where C_{BUS} is the maximum bus capacitance, , and V_{CC} is 3.3V for the NB1A.

With a 100pF load (10 times the DS1337 load), the maximum resistance for 400kHz operation is 3KΩ. For 100kHz the maximum resistance is 10KΩ. If only the DS1337 is on the I^2C bus the maximum resistances would be 100KΩ (100kHz) and 30KΩ (400kHz). The minimum resistance, which is not dependent on bus capacitance, is 966Ω for any operating frequency and C_{BUS}. (Atmel, 2009a)

8.2 DS1337 Interrupt Lines

The DS1337 interrupt lines, `/INTA` and `/INTB` are jumpered to PD6 (Arduino pin 6) and PD5 (Arduino pin 5) respectively. To disconnect `/INTA` cut jumper `J24`. To disconnect `/INTB` cut jumper `J25`. *On boards after revision one* `/INTA` *and* `/INTB` *are also connected to J21 pins one and two. Cutting the J24 and J25 only affects the connection between the DS1337 and the ATmega328. The interrupt lines are always connected to J21.*

There are no pullup resistors connected to the interrupt lines. To use the interrupt lines with the ATmega328 the internal pull-up resistors need to be enabled. For the ATmega328 20KΩ <= R_{pullup} <= 50KΩ which is sufficient to pullup the DS1337 lines. (Atmel, 2009b).

8.3 RTC Battery Life

The DS1337 operates with a V_{CC} from 1.8V to 5.5V. On the NB1A the DS1337 is run off of the CR1220 coin cell which has a capacity of 40mAH (to 2V). The maximum active supply current is 150μA with SCL clocked at 400kHz, The maximum standby current is 1.5μA which is achieved only when the I^2C bus is inactive.(Maxim, 2009a)

With an inactive bus the maximum battery life is ≈ 26000 hours. With an I^2C bus that is run *continuously* the battery life would be ≈ 260 hours. A typical application should have a battery life of one to two years.

9 Quad DAC

The quad DAC on the NB1A is the Texas Instruments TLV5620 which has a resolution of 8 bits. Communication to the DAC is through the SPI interface. The DAC is double buffered allowing all channels to be simultaneously updated. The `LOAD` control line is used to latch data for each individual channel. The `LDAC` control line is used to latch the data from the input latch to the output latch updating all the DAC outputs.

The `LOAD` line is connected to PB0 (Arduino pin 10). The `LDAC` line is connected to PB1 (Arduino pin 9) through jumper `J22`. If simultaneous updates of all channels is not required than `LDAC` can be connected to ground. To ground `LDAC` cut jumper J22 and connect the the `U21` side of `J22` to `J23` (either side).

The reference used is the TLV431B. The reference voltage is 1.24V, ±0.5% (initial accuracy), 50ppm per °C typical drift, 140ppm per °C max drift. Since the NB1A is a 3.3V system the maximum reference is 1.8V (V_{CC} − 1.5V).

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10 Assembly Documentation and Schematics

Table 4: Bill of Materials

Schematic: nb1a_r2.sch Thu Oct 1 14:40:29 2009
BOM: nb1a_r2.bom Thu Oct 1 14:44:19 2009

Qty	Reference	Value	Footprint	Mfg PN
1	B21		CON_BAT__Keystone_500.fp	Keystone 500
6	C1, C2, C3, C4, C13, C21	0.1u	CAPR-254P-318W-508L-660..	Kemet C320C104K5R5TA
2	C5, C9	20p	CAPR-254P-318W-508L-660..	Xicon 140-100N2-200J-RC
2	C10, C11	10uF	CAPPR-200P-500D..	Nichicon UPW1E100MDD
3	C51, C56, C57	0.1u	0805	Kemet C0805C104K5RACTU
1	D3		TO220-3N	On-Semi MBR1545CTG
1	D4		LED-254P-320D..	Kingbright WP7104LGD
1	D6		DO-35.fp	Fairchild 1N4148TA
1	F1		1812	Littelfuse 1812L050PR
1	J1		CON_HDR_RA-254P-13C-2R..	Amp 1-103149-3
2	J3, J9		CON_HDR-254P-3C-1R-3N..	Harwin M20-9990345
1	J5		CON_HDR-254P-6C-1R-6N..	Harwin M20-9990645
1	J6		CON_HDR-254P-3C-2R-6N..	FCI 69192-406HLF
1	J8		CON_HDR_RA-254P-3C-1R-3..	Tyco 5-103765-3
1	J10		CON__CUI_PJ-202AH.fp	CUI PJ-202AH
1	J21		CON_HDR_RA-254P-4C-2R-8..	Amp 103149-4
1	J60		CON_USB_MINI_B..	Molex 67503-1020
1	L1	10uH	IND-1016P-635L-241D..	Bourns 78F100J-RC
1	R1	10K	RES-1016P-630L-240D..	Yageo MFR-25FBF-10K0
1	R2	220	RES-1016P-630L-240D..	Yageo MFR-25FBF-221R
1	R21	200	RES-1016P-630L-240D..	Xicon 271-200/AP-RC
2	R22, R23	4.75K	RES-1016P-630L-240D..	Yageo MFR-25FBF-4K75
1	R58	10K	0805	Yageo 9C08052A1002FKHFT
1	R59	4.7K	0805	Rohm MCR10EZHF4701
1	R62	33K	0805	Yageo 9C08052A3302FKHFT
1	S1		SW..	Panasonic EVQ-PAE04M
1	S2		SW__CK_JS202011CQN.fp	CK JS202011CQN
1	U1		DIP-28-300	Atmel ATmega328P-20PU
1	U4		TO220-3N	On-Semi MC33269T-3.3G
1	U10		SSOP-65P-780L1-28N..	FTDI FT232RL
1	U21		DIP-14-300	TI TLV5620CN
1	U22		TO92-139P.fp	On-Semi TLV431BLPG
1	U23		DIP-8-300	Maxim DS1337+
1	U55		SOT23-95P-280L1-6N..	TI SN65220DBV
1	X1	12MHz	XTAL_HC-49US	ECS ECS-120-20-4X
1	X21	32768	XTAL__Citizen_CFS206.fp	Citizen CFS206-32.768KDZB-UB

Table 5: Component List

Schematic: nb1a_r2.sch Thu Oct 1 14:40:29 2009
BOM: nb1a_r2.bom Thu Oct 1 14:44:19 2009

Reference	Value	Footprint	Mfg PN
B21		CON_BAT__Keystone_500.fp	Keystone 500
C1	0.1u	CAPR-254P-318W-508L-660H..	Kemet C320C104K5R5TA
C2	0.1u	CAPR-254P-318W-508L-660H..	Kemet C320C104K5R5TA
C3	0.1u	CAPR-254P-318W-508L-660H..	Kemet C320C104K5R5TA
C4	0.1u	CAPR-254P-318W-508L-660H..	Kemet C320C104K5R5TA
C5	20p	CAPR-254P-318W-508L-660H..	Xicon 140-100N2-200J-RC
C9	20p	CAPR-254P-318W-508L-660H..	Xicon 140-100N2-200J-RC
C10	10uF	CAPPR-200P-500D..	Nichicon UPW1E100MDD
C11	10uF	CAPPR-200P-500D..	Nichicon UPW1E100MDD
C13	0.1u	CAPR-254P-318W-508L-660H..	Kemet C320C104K5R5TA
C21	0.1u	CAPR-254P-318W-508L-660H..	Kemet C320C104K5R5TA
C51	0.1u	0805	Kemet C0805C104K5RACTU
C56	0.1u	0805	Kemet C0805C104K5RACTU
C57	0.1u	0805	Kemet C0805C104K5RACTU
D3		TO220-3N	On-Semi MBR1545CTG
D4		LED-254P-320D__Kingbright_3mm.fp	Kingbright WP7104LGD
D6		DO-35.fp	Fairchild 1N4148TA
F1		1812	Littelfuse 1812L050PR
J1		CON_HDR_RA-254P-13C-2R-26N..	Amp 1-103149-3
J3		CON_HDR-254P-3C-1R-3N..	Harwin M20-9990345
J5		CON_HDR-254P-6C-1R-6N..	Harwin M20-9990645
J6		CON_HDR-254P-3C-2R-6N..	FCI 69192-406HLF
J8		CON_HDR_RA-254P-3C-1R-3N..	Tyco 5-103765-3
J9		CON_HDR-254P-3C-1R-3N..	Harwin M20-9990345
J10		CON__CUI_PJ-202AH.fp	CUI PJ-202AH
J21		CON_HDR_RA-254P-4C-2R-8N..	Amp 103149-4
J60		CON_USB_MINI_B__Molex_67503-1020	Molex 67503-1020
L1	10uH	IND-1016P-635L-241D..	Bourns 78F100J-RC
R1	10K	RES-1016P-630L-240D..	Yageo MFR-25FBF-10K0
R2	220	RES-1016P-630L-240D..	Yageo MFR-25FBF-221R
R21	200	RES-1016P-630L-240D..	Xicon 271-200/AP-RC
R22	4.75K	RES-1016P-630L-240D..	Yageo MFR-25FBF-4K75
R23	4.75K	RES-1016P-630L-240D..	Yageo MFR-25FBF-4K75
R58	10K	0805	Yageo 9C08052A1002FKHFT
R59	4.7K	0805	Rohm MCR10EZHF4701
R62	33K	0805	Yageo 9C08052A3302FKHFT
S1		SW__Panasonic_EVQPA_Series	Panasonic EVQ-PAE04M
S2		SW__CK_JS202011CQN.fp	CK JS202011CQN
U1		DIP-28-300	Atmel ATmega328P-20PU
U4		TO220-3N	On-Semi MC33269T-3.3G
U10		SSOP-65P-780L1-28N..	FTDI FT232RL
U21		DIP-14-300	TI TLV5620CN
U22		TO92-139P.fp	On-Semi TLV431BLPG
U23		DIP-8-300	Maxim DS1337+
U55		SOT23-95P-280L1-6N__LTC_S6_Package	TI SN65220DBV
X1	12MHz	XTAL_HC-49US	ECS ECS-120-20-4X
X21	32768	XTAL__Citizen_CFS206.fp	Citizen CFS206-32.768KDZB-UB

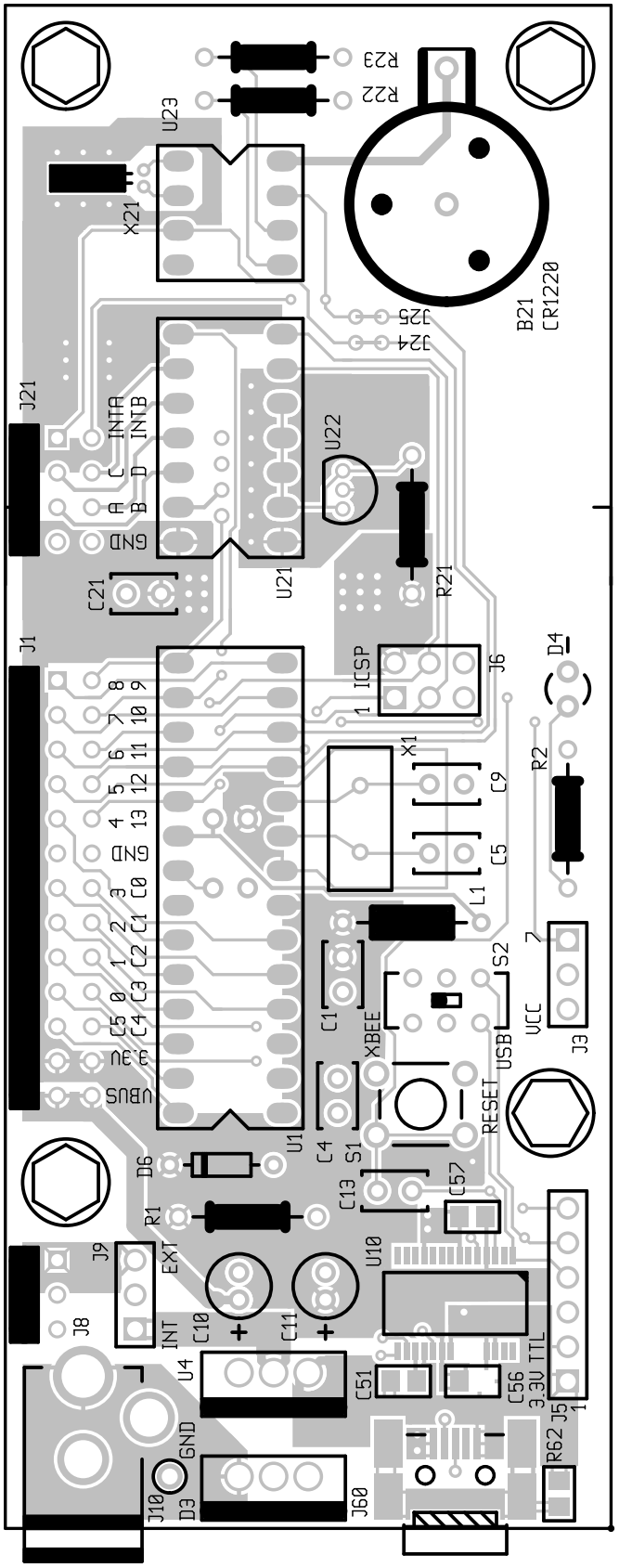


Figure 1: NB1A Top Side Assembly Drawing (Rev 2)

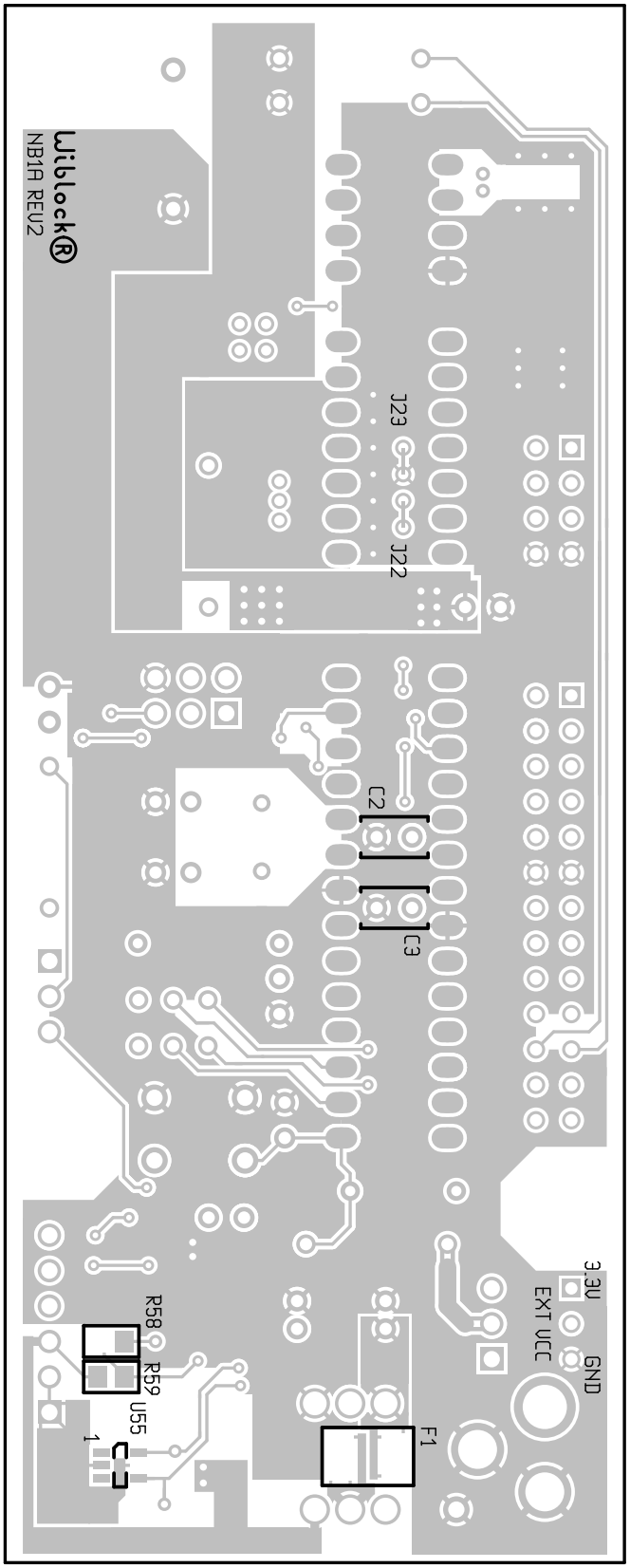


Figure 2: NB1A Bottom Side Assembly Drawing (Rev 2)

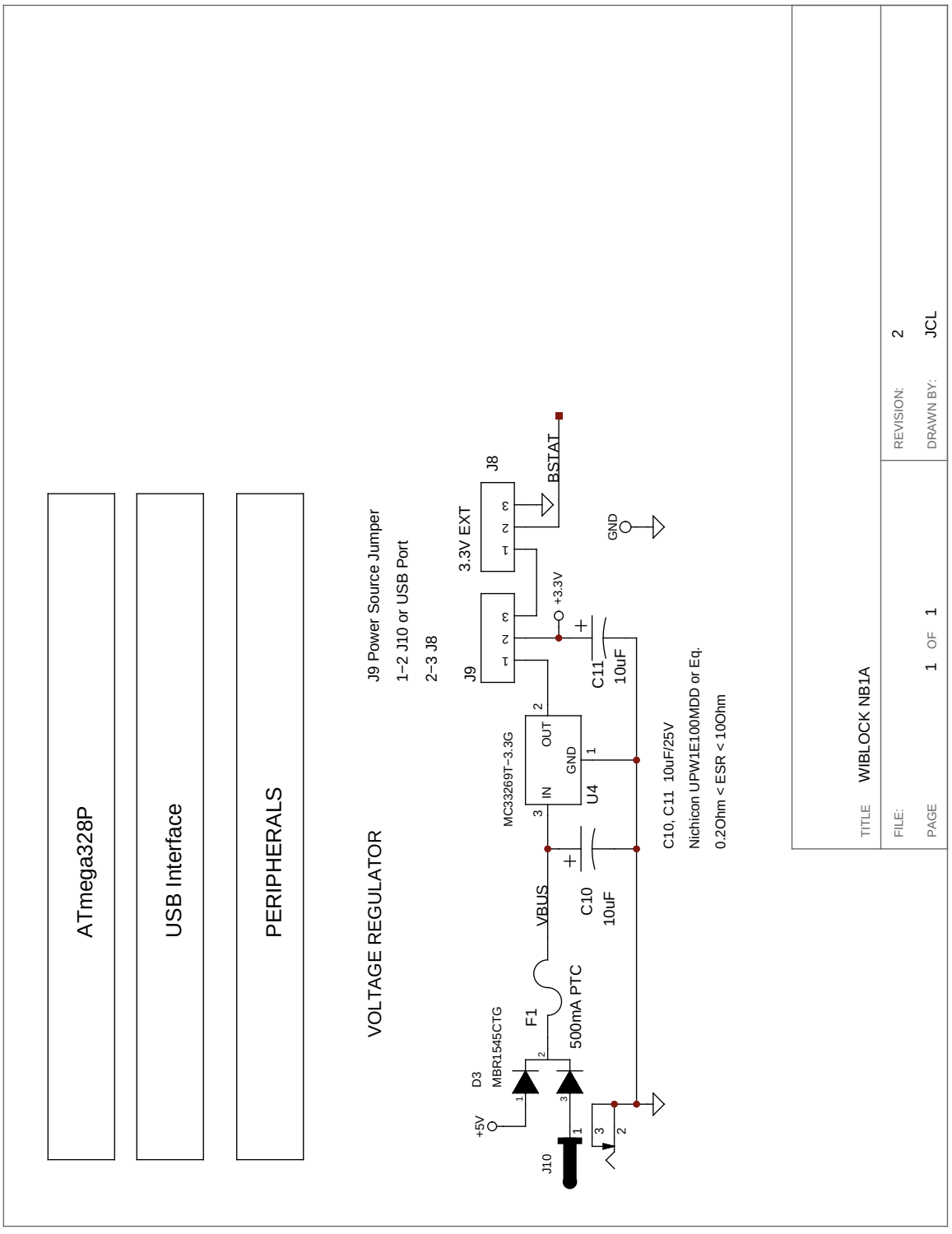


Figure 3: NB1A Top Schematic (Rev 2)

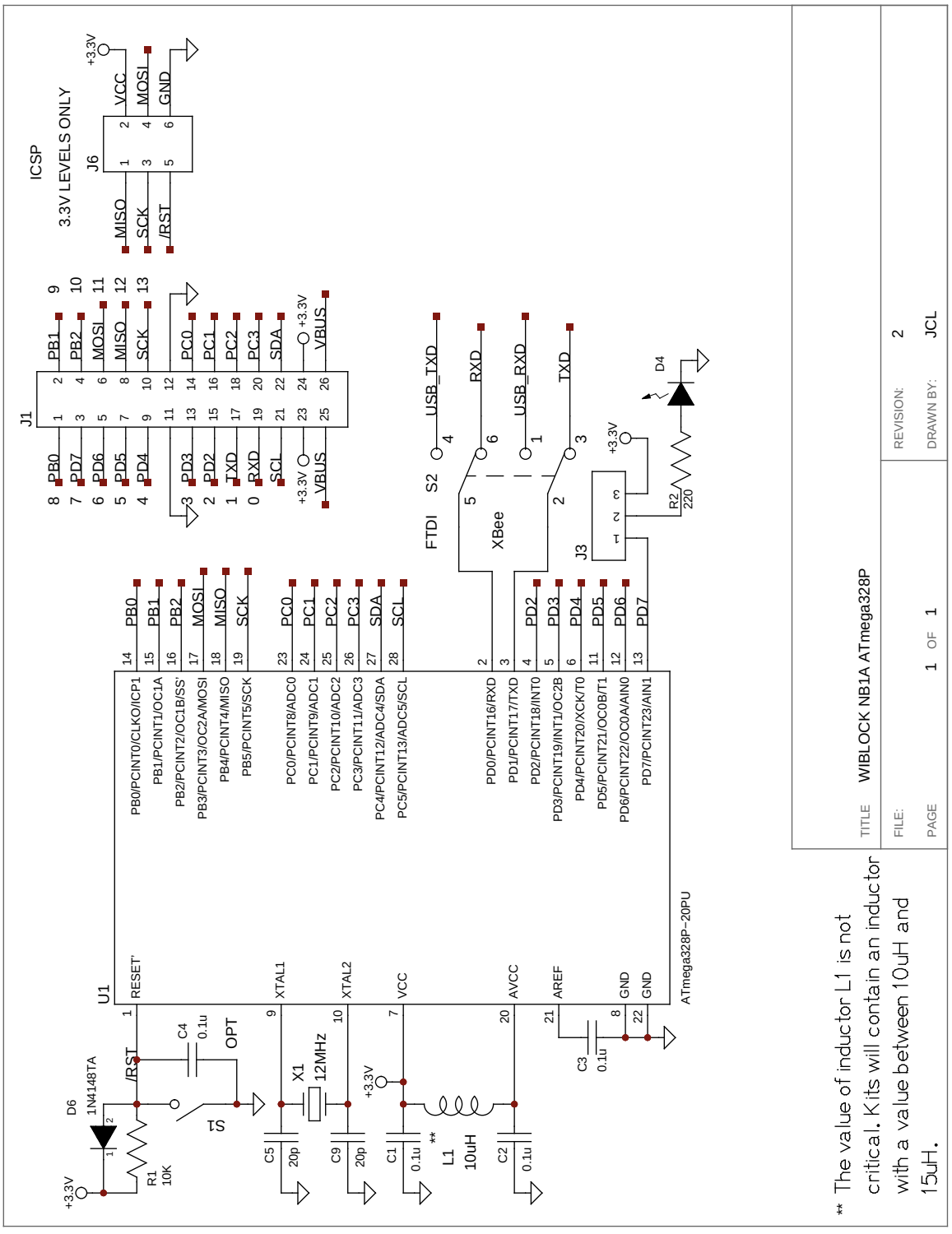


Figure 4: NB1A Microcontroller (Rev 2)

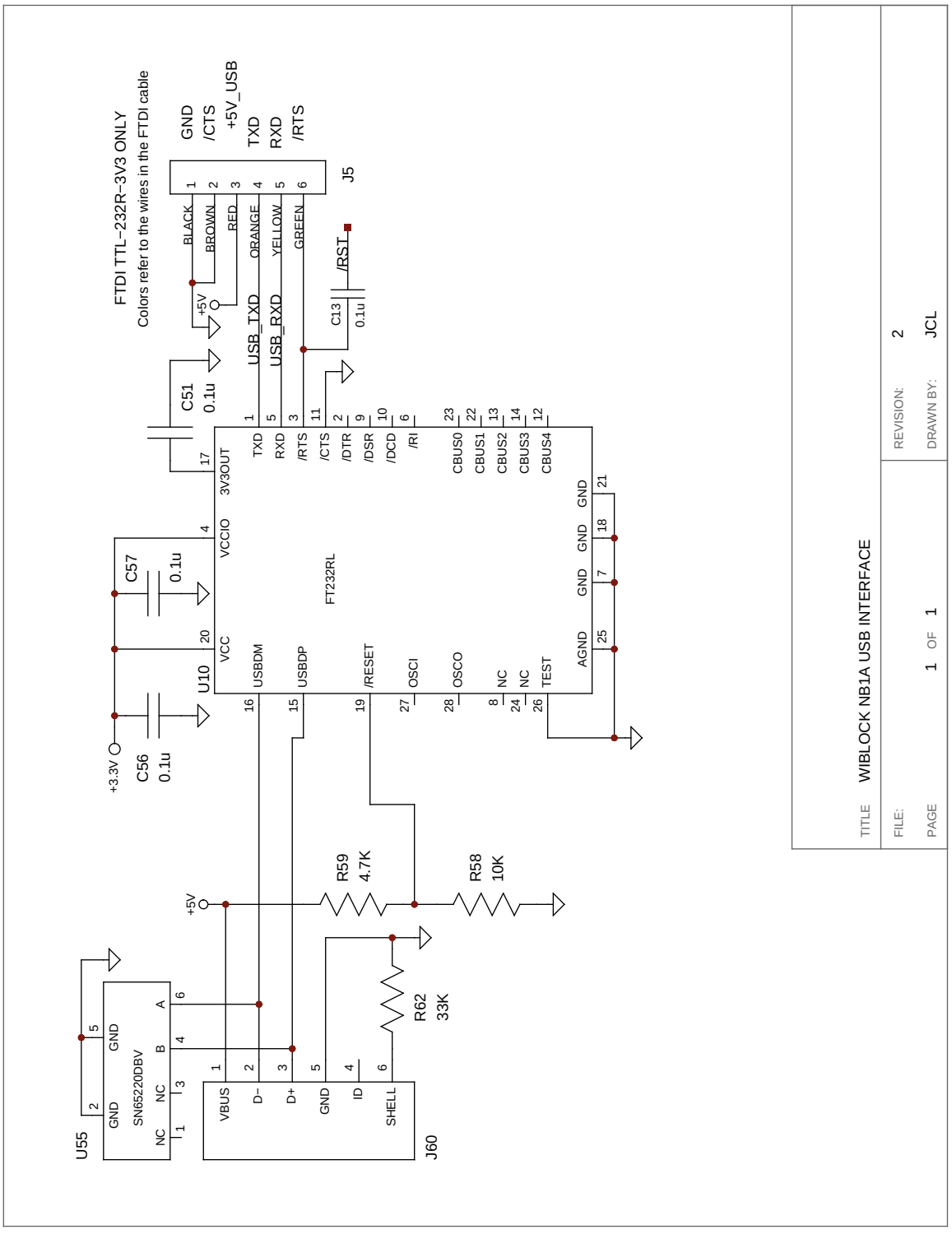


Figure 5: NB1A USB Interface (Rev 2)

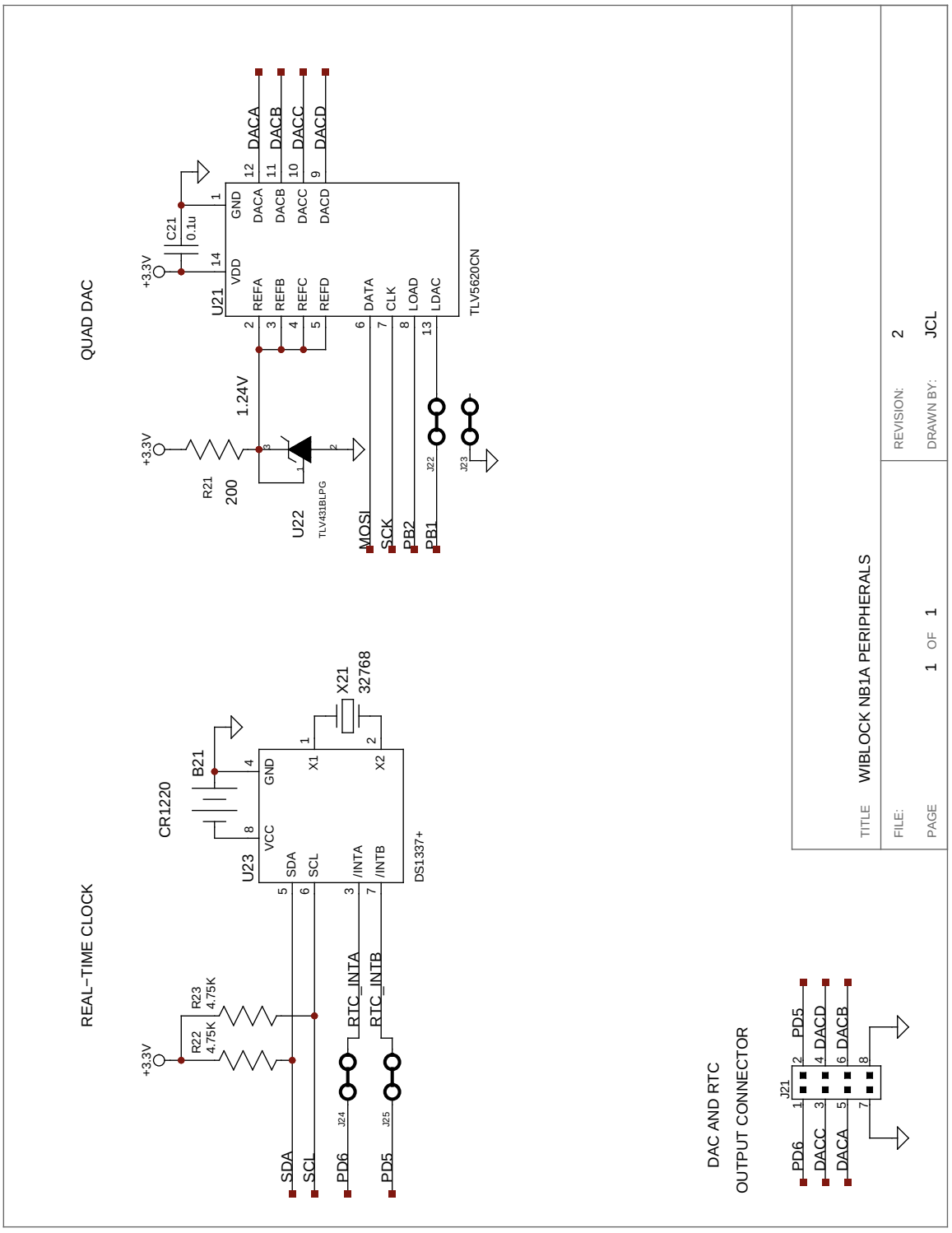


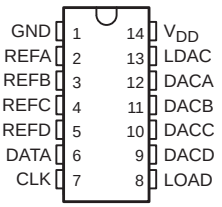
Figure 6: NB1A Peripherals (Rev 2)

TLV5620C, TLV5620I
QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS110B – JANUARY 1995 – REVISED APRIL 1997

- **Four 8-Bit Voltage Output DACs**
- **3-V Single-Supply Operation**
- **Serial Interface**
- **High-Impedance Reference Inputs**
- **Programmable for 1 or 2 Times Output Range**
- **Simultaneous Update Facility**
- **Internal Power-On Reset**
- **Low-Power Consumption**
- **Half-Buffered Output**

D OR N PACKAGE
(TOP VIEW)



applications

- **Programmable Voltage Sources**
- **Digitally Controlled Amplifiers/Attenuators**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLV5620C and TLV5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND; and, the DACs are monotonic. The device is simple to use, because it runs from a single supply of 3 V to 3.6 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLV5620C and TLV5620I is over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises eight bits of data, two DAC select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs update simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high noise immunity.

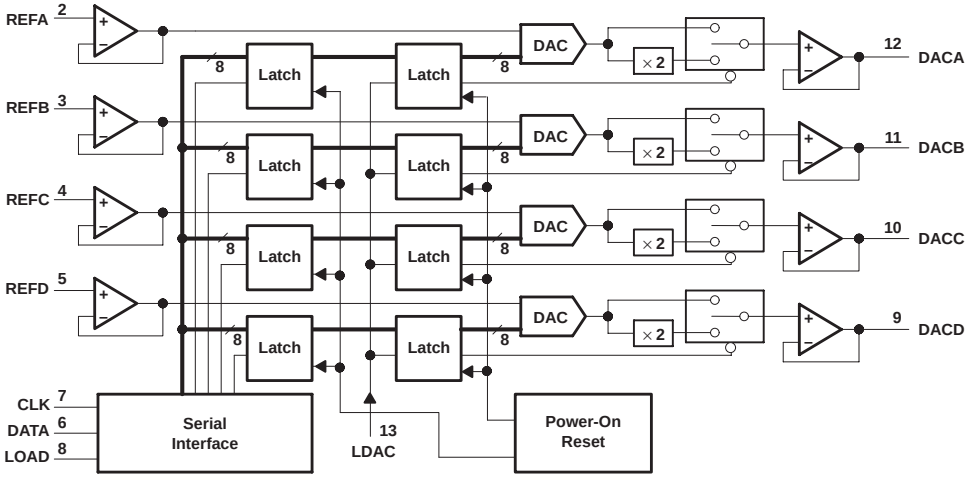
The 14-terminal small-outline (SO) package allows digital control of analog functions in space-critical applications. The TLV5620C is characterized for operation from 0°C to 70°C. The TLV5620I is characterized for operation from –40°C to 85°C. The TLV5620C and TLV5620I do not require external trimming.

AVAILABLE OPTIONS

	PACKAGE	
T_A	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLV5620CD	TLV5620CN
–40°C to 85°C	TLV5620ID	TLV5620IN

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	1	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When this signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	8	I	Serial interface load control. When the LDAC terminal is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REFA	2	I	Reference voltage input to DAC A. This voltage defines the output analog range.
REFB	3	I	Reference voltage input to DAC B. This voltage defines the analog output range.
REFC	4	I	Reference voltage input to DAC C. This voltage defines the analog output range.
REFD	5	I	Reference voltage input to DAC D. This voltage defines the analog output range.
V_{DD}	14	I	Positive supply voltage

detailed description

The TLV5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor segments and upon the performance of the output buffer. Since the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first. Data transfers using two 8-clock-cycle periods are shown in Figures 3 and 4.

Table 2 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

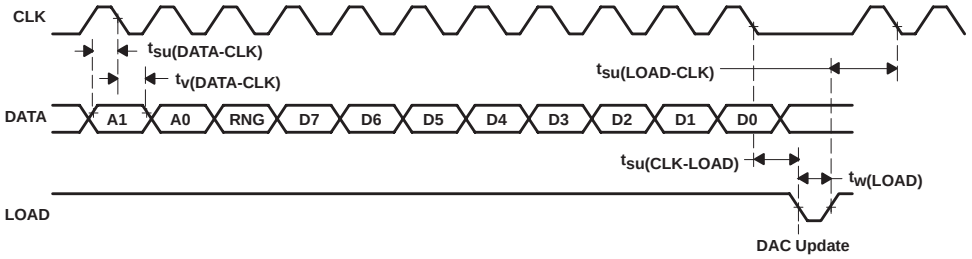


Figure 1. LOAD-Controlled Update (LDAC = Low)

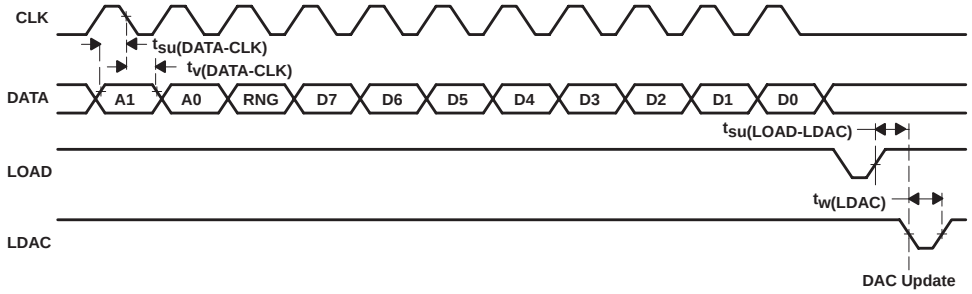


Figure 2. LDAC-Controlled Update

Figure 3. Load Controlled Update Using 8-Bit Serial Word (LDAC = Low)

Figure 4. LDAC Controlled Update Using 8-Bit Serial Word

linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, therefore, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

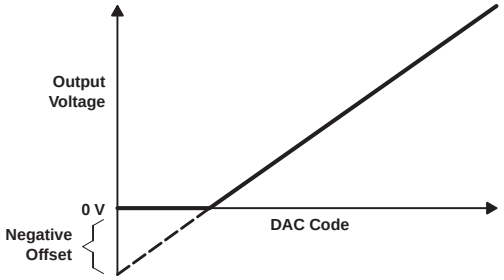
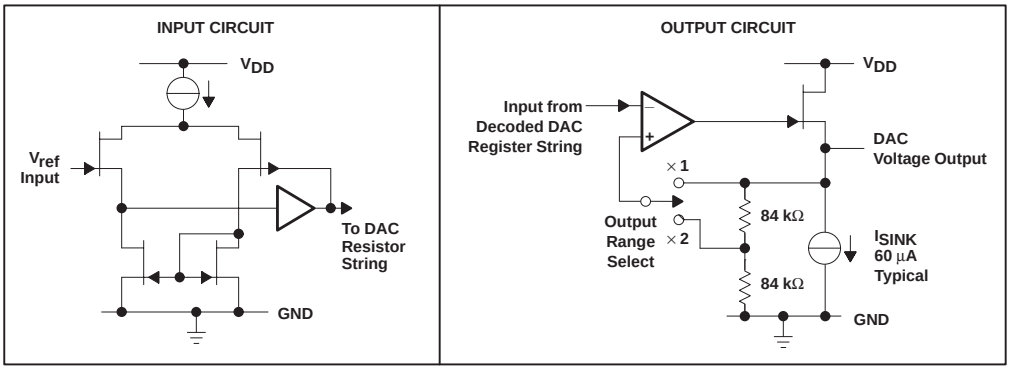


Figure 5. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) . . . . . 7 V
Digital input voltage range . . . . . GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID} . . . . . GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5620C . . . . . 0°C to 70°C
TLV5620I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	3.3	5.25	V
High-level input voltage, V_{IH}		0.8 V_{DD}			V
Low-level input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D], x1 gain				V_{DD}–1.5	V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su(CLK-LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$ (see Figure 2)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLV5620C	0		70	°C
	TLV5620I	–40		85	

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$V_I = V_{DD}$			±10	µA
I_{IL}	Low-level input current	V_I = 0 V			±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output	20			µA
$I_{O(source)}$	Output source current		1			mA
C_i	Input capacitance			15		pF
	Reference input capacitance			15		
I_{DD}	Supply current	V_{DD} = 3.3 V			2	mA
I_{ref}	Reference input current	V_{DD} = 3.3 V, V_{ref} = 1.5 V			±10	µA
E_L	Linearity error (end point corrected)	V_{ref} = 1.25 V, × 2 gain, See Note 1			±1	LSB
E_D	Differential linearity error	V_{ref} = 1.25 V, × 2 gain, See Note 2			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 1.25 V, × 2 gain, See Note 3	0		30	mV
	Zero-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain, See Note 4		10		µV/°C
E_{FS}	Full-scale error	V_{ref} = 1.25 V, × 2 gain, See Note 5			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain, See Note 6		±25		µV/°C
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale error temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the effect of this signal on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varing the V_{DD} voltage from 3 V to 3.6 V dc and measuring the effect of this signal on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF R_L = 10 kΩ		1		V/µs
Output settling time	To ±0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		µs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES: 9. Settling time is the time between a LOAD falling edge and the DAC output reaching full-scale voltage within ± 0.5 LSB starting from an initial output voltage equal to zero.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{PP} and with a digital input code of full-scale.

PARAMETER MEASUREMENT INFORMATION

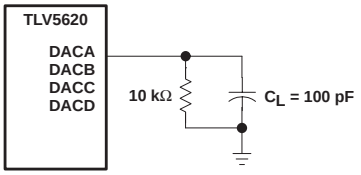
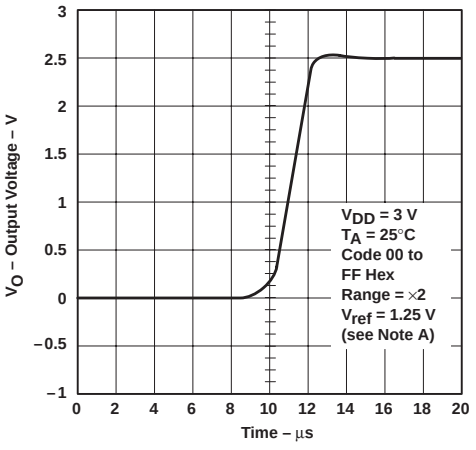


Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS

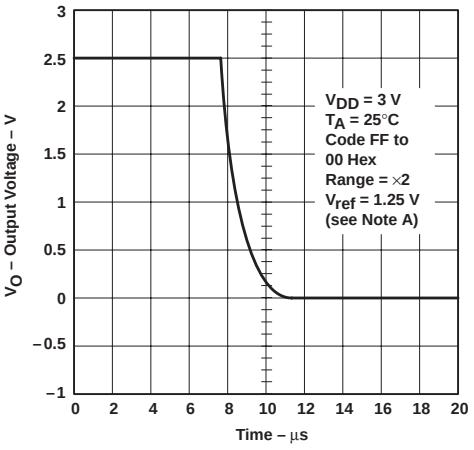
POSITIVE RISE TIME AND SETTLING TIME



NOTE A: Rise time = 2.05 μs, positive slew rate = 0.96 V/μs, settling time = 4.5 μs.

Figure 7

NEGATIVE FALL TIME AND SETTLING TIME



NOTE A: Fall time = 4.25 μs, negative slew rate = 0.46 V/μs, settling time = 8.5 μs.

Figure 8

TYPICAL CHARACTERISTICS

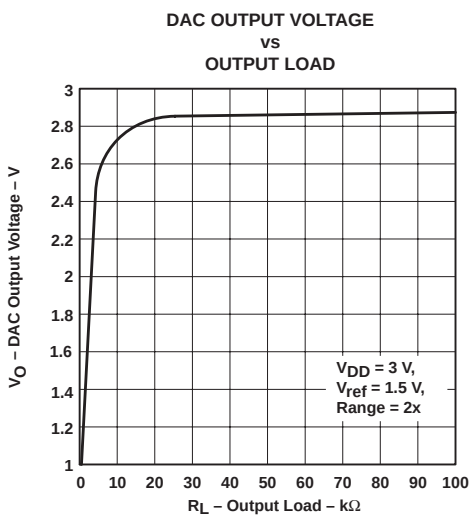


Figure 9

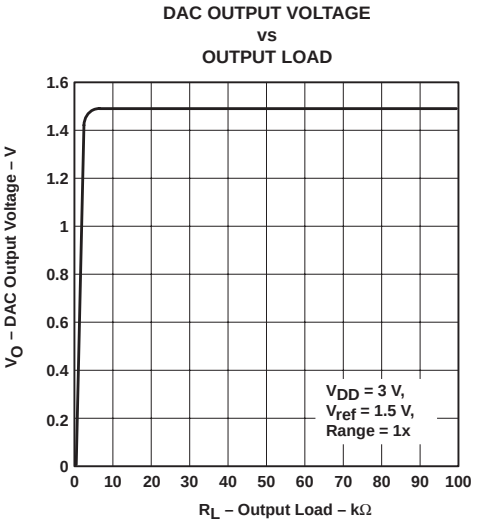


Figure 10

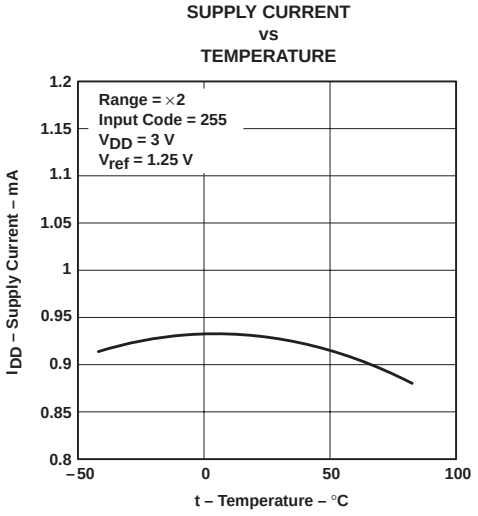
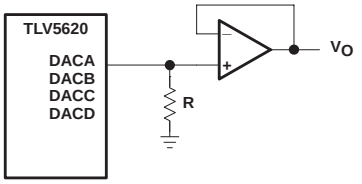


Figure 11

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION



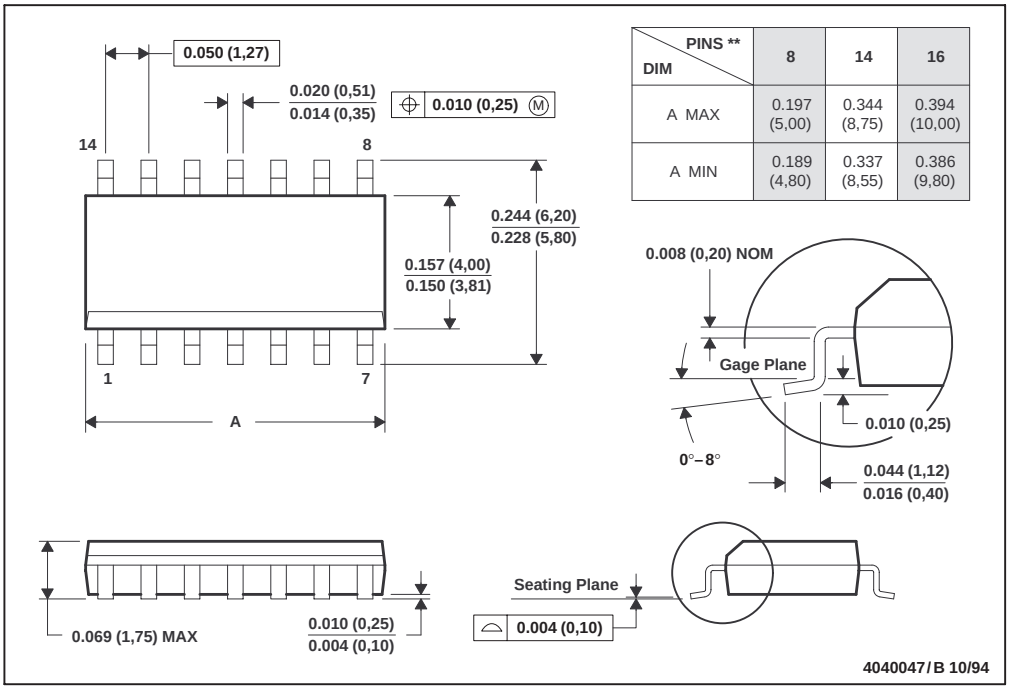
NOTE A: Resistor R ≥ 10 kΩ

Figure 12. Output Buffering Scheme

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad
E. Falls within JEDEC MS-012

TEXAS INSTRUMENTS
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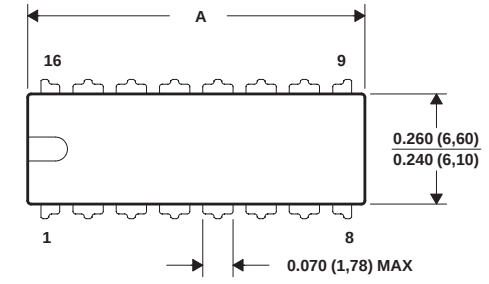
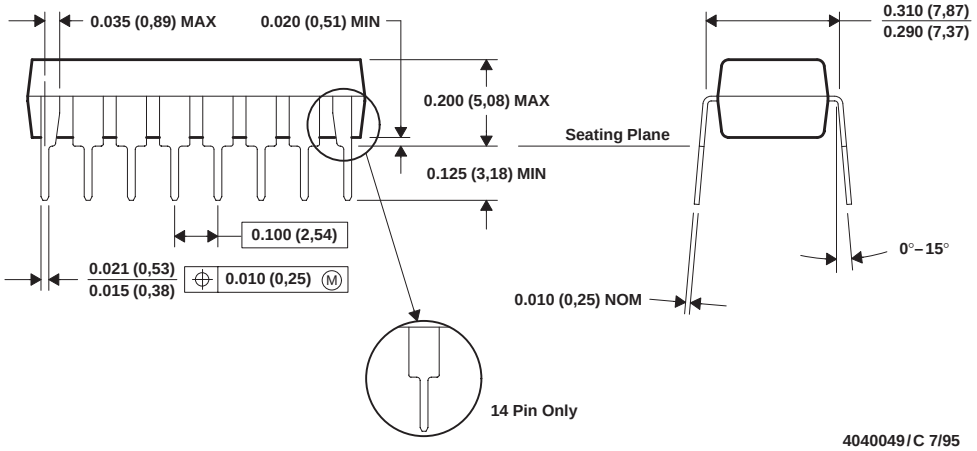
MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV5620CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV5620CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV5620ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV5620IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV5620INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

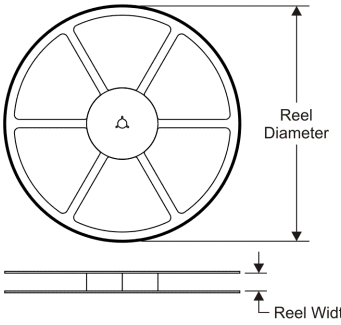
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

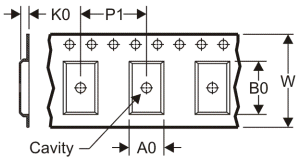
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

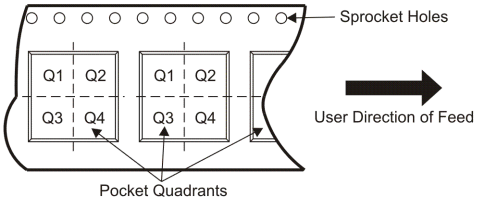


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

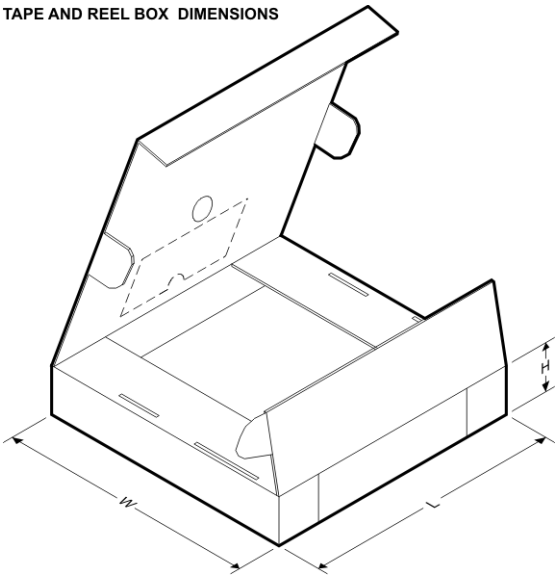
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5620CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV5620IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5620CDR	SOIC	D	14	2500	346.0	346.0	33.0
TLV5620IDR	SOIC	D	14	2500	346.0	346.0	33.0

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Interface	interface.ti.com	Medical	www.ti.com/medical
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		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

19-4652; 7/09

DS1337
I²C Serial Real-Time Clock

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I^2C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The device is fully accessible through the serial interface while V_{CC} is between 1.8V and 5.5V. I^2C operation is not guaranteed below 1.8V. Timekeeping operation is maintained with V_{CC} as low as 1.3V.

APPLICATIONS

Handhelds (GPS, POS Terminal, MP3 Player)

Consumer Electronics (Set-Top Box, VCR/Digital Recording)

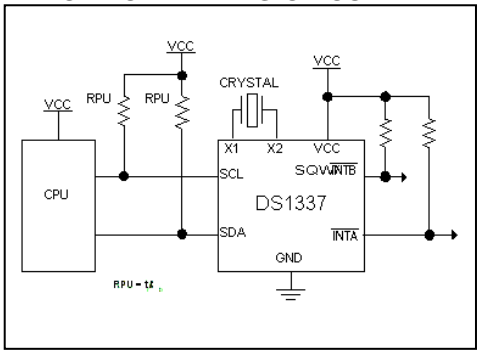
Office Equipment (Fax/Printer, Copier)

Medical (Glucometer, Medicine Dispenser)

Telecommunications (Router, Switch, Server)

Other (Utility Meter, Vending Machine, Thermostat, Modem)

TYPICAL OPERATING CIRCUIT



FEATURES

- **Real-Time Clock (RTC) Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Valid Up to 2100**
- **Available in a Surface-Mount Package with an Integrated Crystal (DS1337C)**
- **I^2C Serial Interface**
- **Two Time-of-Day Alarms**
- **Oscillator Stop Flag**
- **Programmable Square-Wave Output Defaults to 32kHz on Power-Up**
- **Available in 8-Pin DIP, SO, or µSOP**
- **-40°C to +85°C Operating Temperature Range**

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1337+	-40°C to +85°C	8 DIP (300 mils)	DS1337
DS1337S+	-40°C to +85°C	8 SO (150 mils)	DS1337
DS1337U+	-40°C to +85°C	8 µSOP	1337
DS1337C#	-40°C to +85°C	16 SO (300 mils)	DS1337C

+ Denotes a lead(Pb)-free/RoHS-compliant device.
 # Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes.
† A "+" anywhere on the top mark denotes a lead-free device. A "#" denotes a RoHS-compliant device.

Pin Configurations appear at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..….-0.3V to +6.0V
Operating Temperature Range (Noncondensing)……..…….-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	Full operation	1.8	3.3	5.5	V
	V_{CCT}	Timekeeping (Note 5)	1.3		1.8	V
Logic 1	V_{IH}	SCL, SDA	0.7 x V_{CC}		V_{CC} + 0.3	V
		$\overline{INTA}$, SQW/$\overline{INTB}$			5.5	
Logic 0	V_{IL}		-0.3		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS—Full Operation

(**V_{CC} = 1.8V to 5.5V**, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}	(Note 2)	-1		+1	µA
I/O Leakage	I_{LO}	(Note 3)	-1		+1	µA
Logic 0 Output (V_{OL} = 0.4V)	I_{OL}	(Note 3)			3	mA
Active Supply Current	I_{CCA}	(Note 4)			150	µA
Standby Current	I_{CCS}	(Notes 5, 6)			1.5	µA

DC ELECTRICAL CHARACTERISTICS--Timekeeping

(**V_{CC} = 1.3V to 1.8V,** T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timekeeping Current (Oscillator Enabled)	I_{CCTOSC}	(Notes 5, 7, 8, 9)		425	600	nA
Data-Retention Current (Oscillator Disabled)	I_{CCTDDR}	(Notes 5, 9)			100	nA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.8V to 5.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 10)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time (Notes 11, 12)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 13)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 14)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 14)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 14)			400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 15)			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}			100		ms

Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: SCL only.

Note 3: SDA, $\overline{INTA}$, and SQW/$\overline{INTB}$.

Note 4: I_{CCA}—SCL clocking at max frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 5: Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 6: SQW enabled.

Note 7: Specified with the SQW function disabled by setting INTCN = 1.

Note 8: Using recommended crystal on X1 and X2.

Note 9: The device is fully accessible when $1.8 \le V_{CC} \le 5.5V$. Time and date are maintained when $1.3V \le V_{CC} \le 1.8V$.

Note 10: After this period, the first clock pulse is generated

Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 12: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 13: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \ge$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,max} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

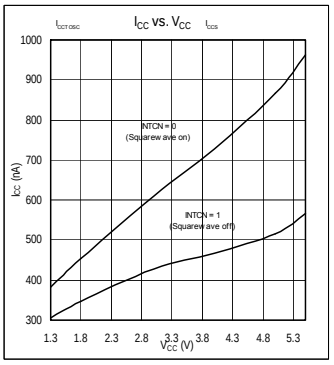
Note 14: C_B—total capacitance of one bus line in pF.

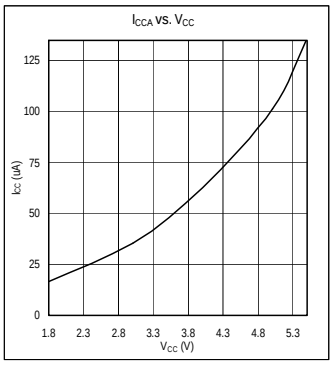
Note 15: Guaranteed by design. Not production tested.

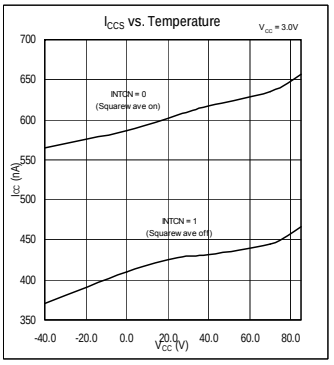
Note 16: The parameter t_{OSF} is the period of time that the oscillator must be stopped for the OSF bit to be set over the voltage range of $V_{CC(MIN)} \le V_{CC} \le V_{CC(MAX)}$.

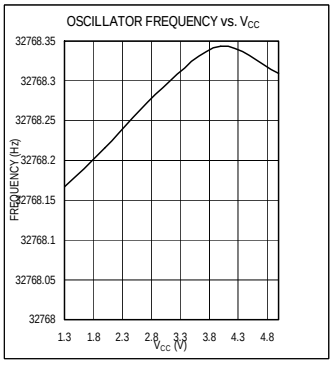
TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)





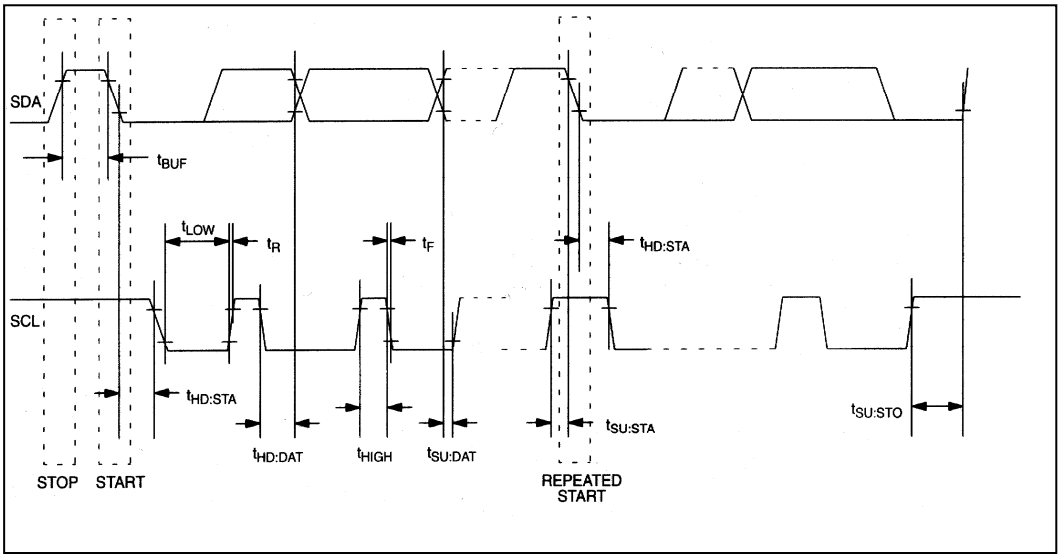




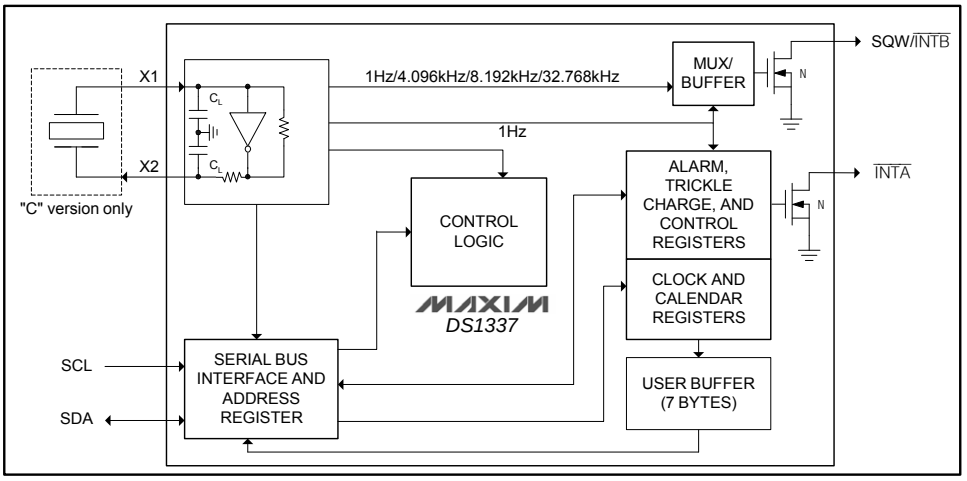
PIN DESCRIPTION

PIN		NAME	FUNCTION
8	16		
1	—	X1	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*. An external 32.768kHz oscillator can also drive the DS1337. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
2	—	X2	
3	14	$\overline{INTA}$	Interrupt Output. When enabled, $\overline{INTA}$ is asserted low when the time/day/date matches the values set in the alarm registers. This pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
4	15	GND	Ground. DC power is provided to the device on this pin.
5	16	SDA	Serial Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is open-drain output and requires an external pullup resistor.
6	1	SCL	Serial Clock Input. SCL is used to synchronize data movement on the serial interface.
7	2	SQW/$\overline{INTB}$	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
8	3	V_{CC}	DC Power. DC power is provided to the device on this pin.
—	4–13	N.C.	No Connect. These pins are not connected internally, but must be grounded for proper operation.

TIMING DIAGRAM



BLOCK DIAGRAM



DETAILED DESCRIPTION

The *Block Diagram* shows the main elements of the DS1337. As shown, communications to and from the DS1337 occur serially over an I²C bus. The DS1337 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible through the I²C interface whenever V_{CC} is between 5.5V and 1.8V. I²C operation is not guaranteed when V_{CC} is below 1.8V. The DS1337 maintains the time and date when V_{CC} is as low as 1.3V.

OSCILLATOR CIRCUIT

The DS1337 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 1. Crystal Specifications*

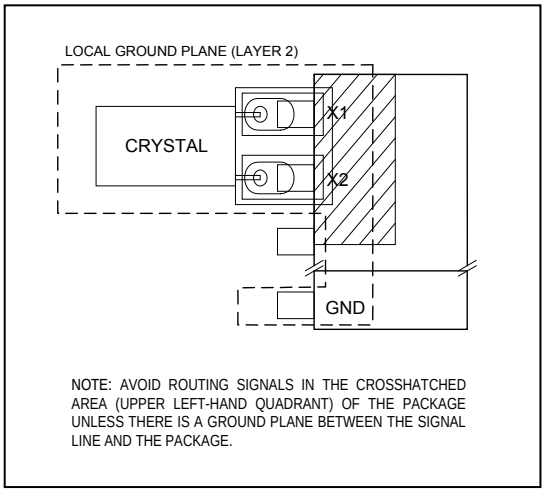
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 1 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Figure 1. Typical PC Board Layout for Crystal



DS1337C ONLY

The DS1337C integrates a standard 32,768Hz crystal in the package. Typical accuracy at nominal V_{CC} and +25°C is approximately +10ppm. Refer to *Application Note 58* for information about crystal accuracy vs. temperature.

OPERATING MODES

The amount of current consumed by the DS1337 is determined, in part, by the I²C interface and oscillator operation. The following table shows the relationship between the operating mode and the corresponding I_{CC} parameter.

Operating Mode	V_{CC}	Power
I²C Interface Active	$1.8V \le V_{CC} \le 5.5V$	I_{CC} Active (I_{CCA})
I²C Interface Inactive	$1.8V \le V_{CC} \le 5.5V$	I_{CC} Standby (I_{CCS})
I²C Interface Inactive	$1.3V \le V_{CC} \le 1.8V$	Timekeeping (I_{CCTOSC})
I²C Interface Inactive Oscillator Disabled	$1.3V \le V_{CC} \le 1.8V$	Data Retention (I_{CCTDDR})

ADDRESS MAP

Table 2 shows the address map for the DS1337 registers. During a multibyte access, when the address pointer reaches the end of the register space (0Fh) it wraps around to location 00h. On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 2. Timekeeper Registers

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Minutes			Minutes				Minutes	00–59
02H	0	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hour				Hours	1–12 +AM/PM 00–23
			10 Hour							
03H	0	0	0	0	0	Day			Day	1–7
04H	0	0	10 Date		Date				Date	01–31
05H	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06H	10 Year				Year				Year	00–99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09H	A1M3	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
			10 Hour							
0AH	A1M4	DY/$\overline{DT}$	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	01–31
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0CH	A2M3	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/PM 00–23
			10 Hour							
0DH	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	01–31
0EH	$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	—

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied or V_{CC} falls below the V_{OSC}.*

I²C INTERFACE

The I²C interface is accessible whenever V_{CC} is at a valid level. If a microcontroller connected to the DS1337 resets while reading from the DS1337 during an I²C read, the two could become unsynchronized. The microcontroller must terminate the last byte read with a Not-Acknowledge (NACK) to properly terminate the read. When the microcontroller resets, the DS1337 I²C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Table 2. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enable, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The DS1337 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). All hours values, including the alarms, must be reinitialized whenever the 12/$\overline{24}$-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99–00.

ALARMS

The DS1337 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h–0Ah. Alarm 2 can be set by writing to registers 0Bh–0Dh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes—each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 3 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. The bit(s) will remain at a logic 1 until written to a logic 0 by the user. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{INTA}$ or SQW/$\overline{INTB}$) signals. The match is tested on the once-per-second update of the time and date registers.

Table 3. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL-PURPOSE REGISTERS

The DS1337 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator ($\overline{EOSC}$). This active-low bit when set to logic 0 starts the oscillator. When this bit is set to logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

SQW/$\overline{INTB}$ Output

INTCN	RS2	RS1	SQW/$\overline{INTB}$ OUTPUT	A2IE
0	0	0	1Hz	X
0	0	1	4.096kHz	X
0	1	0	8.192kHz	X
0	1	1	32.768kHz	X
1	X	X	$\overline{A2F}$	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers l activates the $\overline{INTA}$ pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/$\overline{INTB}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{INTB}$ pin. This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INTA}$ (when INTCN = 0) or to assert SQW/$\overline{INTB}$ (when INTCN = 1). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INTA}$. When the A1IE bit is set to logic 0, the A1F bit does not initiate the $\overline{INTA}$ signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on V_{CC} is insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on either $\overline{INTA}$ or SQW/$\overline{INTB}$ depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the $\overline{INTA}$ pin goes low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the SQW/$\overline{INTB}$ pin goes low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{INTA}$ pin goes low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

I²C SERIAL DATA BUS

The DS1337 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1337 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS1337 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

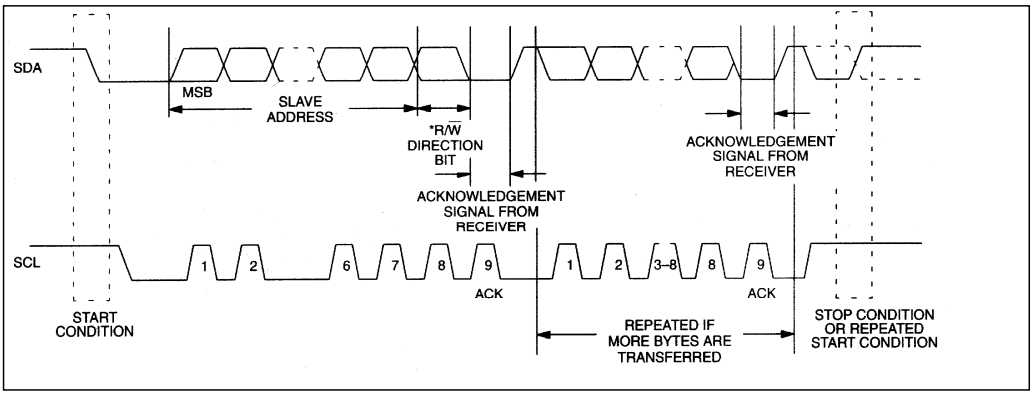
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2. Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1337 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 3). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the DS1337 acknowledges the slave address + write bit, the master transmits a register address to the DS1337. This sets the register pointer on the DS1337. The master may then transmit zero or more bytes of data, with the DS1337 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1337 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 4 and Figure 5). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The DS1337 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1337 must receive a “not acknowledge” to end a read.

Figure 3. Data Write—Slave Receiver Mode

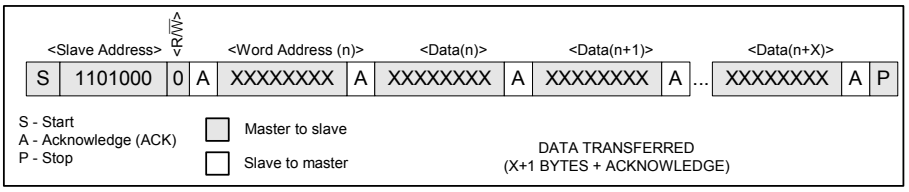


Figure 4. Data Read (from Current Pointer Location)—Slave Transmitter Mode

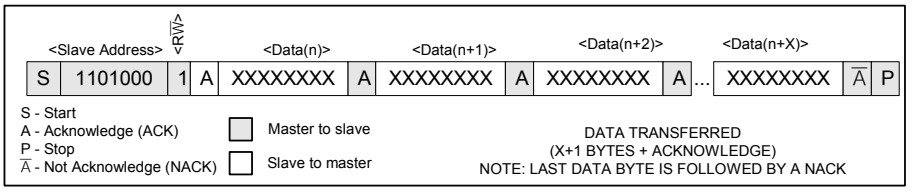
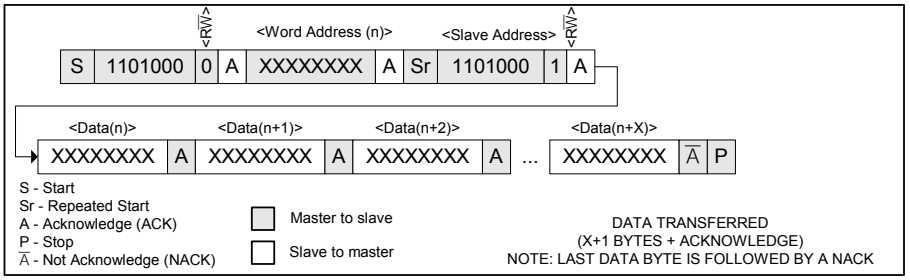


Figure 5. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



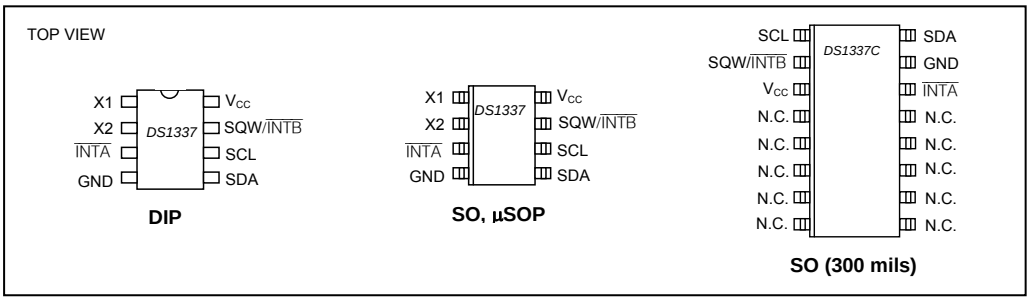
HANDLING, PC BOARD LAYOUT, AND ASSEMBLY

The DS1337C package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

PIN CONFIGURATIONS



CHIP INFORMATION

TRANSISTOR COUNT: 10,950
PROCESS: CMOS

THERMAL INFORMATION

PACKAGE	THETA-J_A (°C/W)	THETA-J_C (°C/W)
8 DIP	110	40
8 SO	170	40
8 µSOP	229	39
16 SO	73	23

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 PDIP	P8+8	**21-0043**
8 SO	S8+2	**21-0041**
8 µMAX	U8+1	**21-0036**
16 SO	W16-H2	**21-0042**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
080508	Added device access details to *General Description* section.	1
	Removed leaded ordering numbers from the *Ordering Information* table.	1
	Added Note 5 to Timekeeping V_{CC} EC table range.	2
	Added “Full Operation” and “Timekeeping” to headers to clarify table usage.	2
	Added OSF parameter to EC table.	3
	Updated *Pin Description* to indicate max input voltage and that unused outputs may be left open.	5
	Added oscillator circuit and show open-drain transistors on *Block Diagram*.	6
	Added *Operating Mode* section with details on operating mode and corresponding Icc parameter.	7
	Added *I²C Interface* section explaining how to synchronize a microcontroller and the RTC.	8
	Corrected legend in figure 5 for not-acknowledge (add overbar to symbol).	14
071609	Removed conflicting SDA/SCL input bias statement in *Pin Description*.	5

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600