

NB1A-LED Description


The NB1A-LED is a 32 channel LED driver that is compatible with the [NB1A](#), [NB1](#), [ZB1](#) and the NB1A backplane. The card is based on the TI TLC5940NT current-sink and works with the Tlc5940 Arduino library.


Each group of 16 channels can be wired using low-cost ribbon cable. Adding additional connectors to a ribbon cable enables groups of channels to be paralleled for increased current capacity.

Features


- 32 independent channels on two 40 pin headers. Compatible with IDE cables.
- Channels can be paralleled using multiple receptacles on a ribbon cable.
- Separate adjustable regulator for the LED drive voltage.
- XLAT can be configured so that multiple cards can be independently controlled on the same bus.
- DCPRG, VPROG and XERR can be configured using jumper wires.
- Compatible with the NB1A, NB1, ZB1 and the NB1A backplane.

1 Assembling the NB1A-LED


 Semiconductors are electrostatic-sensitive devices. Proper ESD handling precautions need to be taken to avoid damage.

 Do not cut any of the U1 socket pins until you have determined which pins are needed in your application. All of the NB1A-LED I/O pins are the U1 socket pins. See ?? for pin removal information.

The Bill of Materials (BOM) and Component List are in [section 6](#). For full page assembly drawings see [Figure 1](#) (top) and [Figure 2](#) (bottom).

 There are two different BOMs and Component Lists – one for the TH kit and one for the SMD kit. The PCB and assembly drawings are common to both kits.

1.1 Power Supply Circuit Assembly

 The NB1A-LED will include a J1 that is either a 20x2 or a 13x2 receptacle. Only the first 13x2 pins are used on the connector. If your kit includes the 13x2 connector align the connector such that pin one is populated. With the board face-up and J1 on the bottom edge and J2, J3 on the top-edge J1 pin 1 is the pin in the lower left corner.

Solder the top side components:


- C10, C11
*C10 and C11 are polarized parts. The long lead is the positive. The short lead is the negative. Make sure that the **positive** lead is inserted into positive hole in the PCB*
- R10
124Ω (brown, red, yellow, black, brown)
- R11
For 3.3V operation this value will be either 205Ω (red, black, green, black, brown) or 210Ω (red, brown, black, black, brown) For 5V operation this value will be 374Ω (orange, violet, yellow, black, brown)
- U10
Make sure that the tab is aligned to the tab marking on the PCB.
- J1
Some kits include a 13x3 receptacle. Only the first 13x2 pins are used on the connector. If your kit includes the 13x2 connector align the connector such that pin one is populated. With the board face-up and J1 on the bottom edge and J2, J3 on the top-edge J1 pin 1 is the pin in the lower left corner.
- C12 (optional, not included)

1.2 LED Drivers

Solder the top side components:

- C2, C3
- R2, R4
10KΩ (brown, black, black, red, brown)
- R3, R5
2KΩ (red, black, black, brown, brown)
- U2, U3 (socket)

1.3 LED Driver Output Connectors

 The NB1A-LED PCB is designed for a 20x2 header connector. Only 34 pins are used (17x2). The connector included in the kit is a 17x2 right-angle header. On each connector only pins 3 - 36 are used. Place the connectors such that the first pin on the header aligns with pin 3 of the PCB layout.

Solder the top side components:

- J2, J2

1.3.1 Using IDE cables

Some IDE cables have a keying pin. If you want to use your NB1A-LED with these cables you need to cut the appropriate pin on J2 and J3.

1.4 IC Installation and Test

1.4.1 U2, U3 (TLC5940)

Remove the TLC5940 drivers from the antistatic foam and insert it into the socket aligning the notch in the IC package with the notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

2 IO Connectors

J1 20x2 input receptacle.

J2 17x2 U2 outputs (footprint will accept an 18x2, 19x2 or 20x2 header).

J3 17x2 U3 outputs (footprint will accept an 18x2, 19x2 or 20x2 header).

3 Electrical Hints

3.1 LED Drive Currents

The NB1A-LED operates of of the 3.3V supply from the NB1A, NB1, or ZB1. This limits the current per channel to 60mA. Changing the LDO on the NB1A, NB1 or ZB1 to a 5V output enables currents of 120mA per channels.

⚠ Besides the current per channel current limitation the TLC5940 is limited by power dissipation. Trimming the LED voltage regulator (U10) will minimize the power dissipation in the TLC5940. See [subsection 3.2](#).

absolute maximum current per channel 130mA

maximum power ($T_A = 25^\circ\text{C}$) 2.4W(derating for T_A 25°C is 27.86mWper °C)

maximum power ($T_A = 85^\circ\text{C}$) 1.8W

maximum LDO current 800mA(see [3.2](#))

3.2 Trimming VLED

To reduce the amount of power dissipated in U2 and U3 an adjustable LDO (U10) has been added to the NB1A-LED. U10 is connected to the LED anodes. U10 should

The input voltage is limited by the amount of power dissipated in the LDO regulator (U10). This varies by application.

⚠ It is critical to keep the power dissipation in the LDO regulator (U10), to less than one watt. The voltage drop across U10 is

$$V_{drop} = V_{bus} - V_{led}$$

Where V_{bus} is the bus voltage from the NB1A, NB1 and or ZB1 that is connected to the NB1A-LED and V_{led} is the output voltage of U10 (see [subsection 3.3](#)). The power dissipated in U10 is given by

$$P_{diss} = V_{drop} \cdot I_{LED}$$

where I_{LED} is the total current out of U10. The total current out of U10 is the sum of all the currents into U2 and U3. Which is –

$$I_{LED} = \text{numberofchannelson} \cdot I_{set}$$

where I_{set} is the current setting of U2 and U3.

3.3 Changing V_{cc}

V_{cc} , which is the output of the MC33269T regulator, is adjusted by changing the value of R11. The equation for V_{cc} is –

$$V_{cc} = 1.24 \cdot \frac{124 + R_{11}}{124}$$

R_{11} values for common output voltages are listed in [Table 1](#). The NB1A-LED kits come with both values listed in the table.

V_{cc} (volts)	R_{11} (ohms)	R_2 (ohms)
3.3	205	374
5.0	374	1000

Table 1: R_{11} and R_2 values for 3.3V and 5V Operation

3.3.1 Calculating LDO Junction Temperature

The power dissipation in the LDO (SMD or TH) is

$$P_{diss} = V_{drop} \cdot I_{LED}$$

where

$$V_{drop} = V_{bus} - V_{LED}$$

and

V_{bus} is the input voltage to the NB1A-LED

V_{LED} is the output voltage of the LDO regulator (U10)

I_{LED} is the total current of all U2 and U3 channels that are on.

The junction temperature of the LDO is

$$T_J = P_{DISS} \cdot R_{\theta JA} + T_{AMBIENT}$$

where

$R_{\theta JA}$ is the thermal resistance of the LDO regulator (U10) (70°C/W).

$T_{AMBIENT}$ is the ambient temperature that the NB1A-LED is operating at.

4 IREF

Adjusting the current per channel.

5 Jumper Options

The board can be programmed using the Tlc5940 without changing any jumpers. Since there are two TLC5940 drivers daisy-chained on the NB1A-LED the constant `NUM_TLCS` in `tlc_config.h` needs to be changed from 1 to 2.

Listing 1: Changing the number of TLCs

```
// The NB1A-LED has two TLC
// drivers — U2 and U3

#define NUM_TLCS      2
```

5.1 DCPRG

The `DCPRG` pin switches the dot correction data input. When `DCPRG` = low DC is connected to the EEPROM. When `DCPRG` = high DC is connected to the DC register.

5.2 VPRG

When `VPRG` is low the TLC5940 is in grayscale (GS) mode. Data is transferred to the GS register. When `VPRG` is high the TLC5940 is in dot-correction (DC) mode.

5.3 XERR

The open-drain `XERR` output is used to report both of the TLC5940 error flags, thermal error flag (`TEFF`) and LED

open detection (`LOD`). During normal operation the `XERR` output floats. Either `TEFF` or `LOD` will pull `XERR` low.

If the TLC5940 junction temperature exceeds the threshold temperature (typically 160°C) `TEFF` goes high and `XERR` goes low. If the LED-open detector detects a broken or disconnected LED `LOD` goes high and `XERR` goes low.

`XERR` can be connected to microcontroller pins PD7 (J8), PD6 (J9), PD5 (J10), PD4 (J11) using the open jumpers.

5.4 BLANK

When `BLANK` is high all outputs are forced off and the grayscale counter (GS) is reset. When `BLANK` is low all outputs are controlled by the grayscale PWM counter. On the NB1A-LED, both the U2 and U3 `BLANK` pins are connected to PB2. If jumper J6 is cut the `BLANK` pin on U3 can be jumpered to PB0 (J5), PD7 (J8), PD6 (J9), PD5 (J10), PD4 (J11).

5.5 XLAT

`XLAT` is a level-triggered latch signal. When `XLAT` is high the TLC5940 writes data from the input shift register to either the GS register (`VPRG` = low) or DC register (`VPRG` = high). `VPRG` on the NB1A-LED is jumpered to GND (low). This can be changed by cutting jumper J14 (U2) and J12 (U3) (See subsection 5.2)

References

- Atmel. (2009). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash.
(Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)
- Maxim. (2009, July). DS1337 I2C Serial Real-Time Clock.
(Retrieved September 30, 2009, from <http://datasheets.maxim-ic.com/en/ds/DS1337-DS1337C.pdf>)

6 Assembly Documentation and Schematics

Table 2: Bill of Materials

Kit: NB1A-LED-KIT

Qty	Reference	Part Number	Description
2	C10, C11	CAPPR_Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
3	C2, C3, C12	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
1	J1	HDRF_RA-20x2-100M	header, female, RA, 20x2, 100mils
2	R2, R4	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
2	R3, R5	RES-2K00-0W125-1T00	resistor, 2.0K, 1/8W, 1%
1	R10	RES-124R-0W125-1T00	resistor, 124 Ohm, 1/8W, 1%
1	R11	RES-205R-0W125-1T00	resistor, 205 Ohm, 1/8W, 1%
2	U2, U3	IC_DAC_TL_TLC5940NT	IC, LED Driver, TLC5940NT, 32ch
1	U10	VREG_On-Semi_MC33269TG	voltage regulator, adj, 800mA, TO-220
2		DIP-28P-300M	DIP Socket, 28 Pin, 300mil centers
2		wiblock_HDR_RA_BR-17X2-100M	
1		wiblock_NB1A-LED-PCB	

Table 3: Component List

Kit: NB1A-LED-KIT

Reference	Part Number	Description
C10	CAPPR_Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
C11	CAPPR_Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
C2	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C3	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C12	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
J1	HDRF_RA-20x2-100M	header, female, RA, 20x2, 100mils
R2	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R4	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R3	RES-2K00-0W125-1T00	resistor, 2.0K, 1/8W, 1%
R5	RES-2K00-0W125-1T00	resistor, 2.0K, 1/8W, 1%
R10	RES-124R-0W125-1T00	resistor, 124 Ohm, 1/8W, 1%
R11	RES-205R-0W125-1T00	resistor, 205 Ohm, 1/8W, 1%
U2	IC_DAC_TL_TLC5940NT	IC, LED Driver, TLC5940NT, 32ch
U3	IC_DAC_TL_TLC5940NT	IC, LED Driver, TLC5940NT, 32ch
U10	VREG_On-Semi_MC33269TG	voltage regulator, adj, 800mA, TO-220
	DIP-28P-300M	DIP Socket, 28 Pin, 300mil centers
	wiblock_HDR_RA_BR-17X2-100M	
	wiblock_NB1A-LED-PCB	

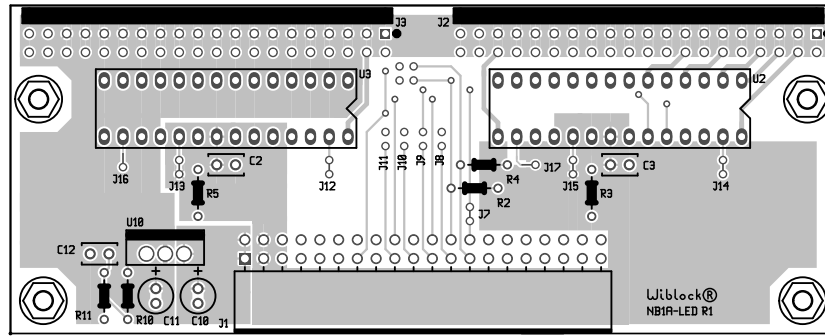


Figure 1: NB1A-LED Top Side Assembly Drawing (Rev 1)

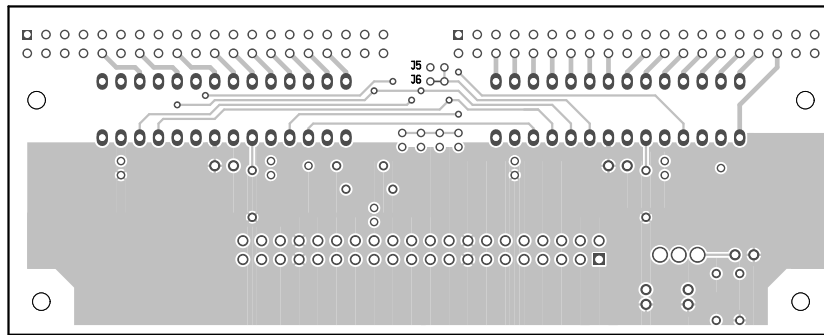


Figure 2: NB1A-LED Bottom Side Assembly Drawing (Rev 1)





16 CHANNEL LED DRIVER WITH DOT CORRECTION AND GRayscale PWM CONTROL

FEATURES

- 16 Channels
- 12 bit (4096 Steps) Grayscale PWM Control
- Dot Correction
 - 6 bit (64 Steps)
 - Storable in Integrated EEPROM
- Drive Capability (Constant-Current Sink)
 - 0 mA to 60 mA ($V_{CC} < 3.6$ V)
 - 0 mA to 120 mA ($V_{CC} > 3.6$ V)
- LED Power Supply Voltage up to 17 V
- $V_{CC} = 3$ V to 5.5 V
- Serial Data Interface
- Controlled In-Rush Current
- 30MHz Data Transfer Rate
- CMOS Level I/O
- Error Information
 - LOD: LED Open Detection
 - TEF: Thermal Error Flag

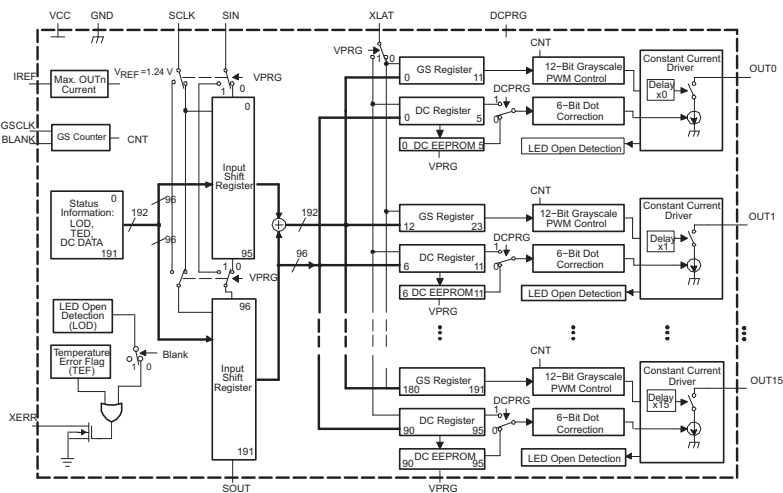
APPLICATIONS

- Monocolor, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Backlighting
- General, High-Current LED Drive

DESCRIPTION

The TLC5940 is a 16-channel, constant-current sink LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step, constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. The dot correction data is stored in an integrated EEPROM. Both grayscale control and dot correction are accessible via a serial interface. A single external resistor sets the maximum current value of all 16 channels.

The TLC5940 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾	PART NUMBER
–40°C to 85°C	28-pin HTSSOP PowerPAD™	TLC5940PWP
	32-pin 5mm x 5mm QFN	TLC5940RHB
	28-pin PDIP	TLC5940NT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS.

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
V _I	Input voltage range ⁽²⁾	VCC
I _O	Output current (dc)	130mA
V _I	Input voltage range	V _(BLANK) , V _(DCPRG) , V _(SCLK) , V _(XLAT) , V _(SIN) , V _(GSCLK) , V _(IREF)
V _O	Output voltage range	V _(SOUT) , V _(XERR)
		V _(OUT0) to V _(OUT15)
	EEPROM program range	V _(VPRG)
	EEPROM write cycles	50
	ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)
		CBM (JEDEC JESD22-C101, Charged Device Model)
T _{stg}	Storage temperature range	–55°C to 150°C
T _A	Operating ambient temperature range	–40°C to 85°C
Package thermal impedance ⁽³⁾	HTSSOP (PWP) ⁽⁴⁾	31.58°C/W
	QFN (RHB)	35.9°C/W
	PDIP (NP)	48°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

(4) With PowerPAD soldered on PCB with 2 oz. (56.7 grams) trace of copper. See SLMA002 for further information.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V _{CC}	Supply Voltage		3		5.5	V
V _O	Voltage applied to output (OUT0–OUT15)				17	V
V _{IH}	High-level input voltage		0.8 V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage		GND		0.2 V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 5V at SOUT			–1	mA
I _{OL}	Low-level output current	V _{CC} = 5V at SOUT, XERR			1	mA
I _{OLC}	Constant output current	OUT0 to OUT15, V _{CC} < 3.6V			60	mA
		OUT0 to OUT15, V _{CC} > 3.6V			120	mA
V _(VPRG)	EEPROM program voltage		20	22	23	V
T _A	Operating free-air temperature range		–40		85	°C
AC CHARACTERISTICS						
V _{CC} = 3 V to 5.5 V, T _A = –40°C to 85°C (unless otherwise noted)						
f _(SCLK)	Data shift clock frequency	SCLK			30	MHz
f _(GSCLK)	Grayscale clock frequency	GSCLK			30	MHz
t _{wh0} /t _{wl0}	SCLK pulse duration	SCLK = H/L (see Figure 11)	16			ns
t _{wh1} /t _{wl1}	GSCLK pulse duration	GSCLK = H/L (see Figure 11)	16			ns
t _{wh2}	XLAT pulse duration	XLAT = H (see Figure 11)	20			ns
t _{wh3}	BLANK pulse duration	BLANK = H (see Figure 11)	20			ns
t _{su0}	Setup time	SIN to SCLK ↑ ⁽¹⁾ (see Figure 11)	5			ns
t _{su1}		SCLK ↓ to XLAT ↑ (see Figure 11)	10			ns
t _{su2}		VPRG ↑ ↓ to SCLK ↑ (see Figure 11)	10			ns
t _{su3}		VPRG ↑ ↓ XLAT ↑ (see Figure 11)	10			ns
t _{su4}		BLANK ↓ to GSCLK ↑ (see Figure 11)	10			ns
t _{su5}		XLAT ↑ to GSCLK ↑ (see Figure 11)	30			ns
t _{su6}	Hold Time	VPRG ↑ to DCPRG ↑ (see Figure 16)	1			ms
t _{h0}		SCLK ↑ to SIN (see Figure 11)	3			ns
t _{h1}		XLAT ↓ to SCLK ↑ (see Figure 11)	10			ns
t _{h2}		SCLK ↑ to VPRG ↑ ↓ (see Figure 11)	10			ns
t _{h3}		XLAT ↓ to VPRG ↑ ↓ (see Figure 11)	10			ns
t _{h4}		GSCLK ↑ to BLANK ↑ (see Figure 11)	10			ns
t _{h5}		DCPRG ↓ to VPRG ↓ (see Figure 11)	1			ms
t _{prog}	Programming time for EEPROM (see Figure 16)		20			ms

(1) ↑ and ↓ indicates a rising edge, and a falling edge respectively.

DISSIPATION RATINGS

PACKAGE	POWER RATING T _A < 25°C	DERATING FACTOR ABOVE T _A = 25°C	POWER RATING T _A = 70°C	POWER RATING T _A = 85°C
28-pin HTSSOP with PowerPAD™ ⁽¹⁾ soldered	3958mW	31.67mW/°C	2533mW	2058mW
28-pin HTSSOP with PowerPAD™ unsoldered	2026mW	16.21mW/°C	1296mW	1053mW
32-pin QFN ⁽¹⁾	3482mW	27.86mW/°C	2228mW	1811mW
28-pin PDIP	2456mW	19.65mW/°C	1572mW	1277mW

(1) The PowerPAD is soldered to the PCB with a 2 oz. (56.7 grams) copper trace. See [SLMA002](#) for further information.

ELECTRICAL CHARACTERISTICSV_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1mA, SOUT	V _{CC} -0.5			V
V _{OL}	Low-level output voltage	I _{OL} = 1mA, SOUT			0.5	V
I _I	Input current	V _I = V _{CC} or GND; BLANK, DCPRG, GSCLK, SCLK, SIN, XLAT	-1		1	μA
		V _I = GND; VPRG	-1		1	
		V _I = V _{CC} ; VPRG			50	mA
		V _I = 22V; VPRG; DCPRG = V _{CC}		4	10	
I _{CC}	Supply current	No data transfer, all output OFF, V _O = 1V, R _(IREF) = 10kΩ		0.9	6	mA
		No data transfer, all output OFF, V _O = 1V, R _(IREF) = 1.3kΩ		5.2	12	
		Data transfer 30MHz, all output ON, V _O = 1V, R _(IREF) = 1.3kΩ		16	25	
		Data transfer 30MHz, all output ON, V _O = 1V, R _(IREF) = 640Ω		30	60	
I _{O(LC)}	Constant sink current (see Figure 2)	All output ON, V _O = 1V, R _(IREF) = 640Ω	54	61	69	mA
I _{kg}	Leakage output current	All output OFF, V _O = 15V, R _(IREF) = 640Ω, OUT0 to OUT15			0.1	μA
ΔI _{O(LC0)}	Constant sink current error (see Figure 2)	All output ON, V _O = 1V, R _(IREF) = 640Ω, OUT0 to OUT15, -20°C to 85°C		1	±4	%
		All output ON, V _O = 1V, R _(IREF) = 640Ω, OUT0 to OUT15 ⁽¹⁾		1	8	
		All output ON, V _O = 1V, R _(IREF) = 320Ω, OUT0 to OUT15, -20°C to 85°C		1	6	
		All output ON, V _O = 1V, R _(IREF) = 320Ω, V _{CC} = 4.5V to 5.5V, OUT0 to OUT15 ⁽¹⁾	±1	±8		
ΔI _{O(LC1)}	Constant sink current error (see Figure 2)	Device to device, Averaged current from OUT0 to OUT15, R _(IREF) = 1920Ω (20mA) ⁽²⁾	-2 +0.4		4	%
ΔI _{O(LC2)}	Constant sink current error (see Figure 2)	Device to device, Averaged current from OUT0 to OUT15, R _(IREF) = 480Ω (80mA) ⁽²⁾	-2.7 +2		±4	%
ΔI _{O(LC3)}	Line regulation (see Figure 2)	All output ON, V _O = 1V, R _(IREF) = 640Ω OUT0 to OUT15, V _{CC} = 3V to 5.5V ⁽³⁾		1	±4	%/V
		All output ON, V _O = 1V, R _(IREF) = 320Ω , OUT0 to OUT15, V _{CC} = 3V to 5.5V ⁽³⁾		±1	±6	%/V
ΔI _{O(LC4)}	Load regulation (see Figure 2)	All output ON, V _O = 1V to 3V, R _(IREF) = 640Ω, OUT0 to OUT15 ⁽⁴⁾		±2	±6	%/V
		All output ON, V _O = 1V to 3V, R _(IREF) = 320Ω, OUT0 to OUT15 ⁽⁴⁾		2	8	%/V
T _(TEF)	Thermal error flag threshold	Junction temperature ⁽⁵⁾	150		170	°C
V _(LED)	LED open detection threshold			0.3	0.4	V
V _(IREF)	Reference voltage output	R _(IREF) = 640Ω	1.20	1.24	1.28	V

(1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by Equation 1 in Table 1.

(2) The deviation of average of OUT1-15 constant current from the ideal constant-current value. It is calculated by Equation 2 in Table 1.

(3) The ideal current is calculated by Equation 3 in Table 1.

(4) The line regulation is calculated by Equation 4 in Table 1.

(5) The load regulation is calculated by Equation 5 in Table 1.

(6) Not tested. Specified by design

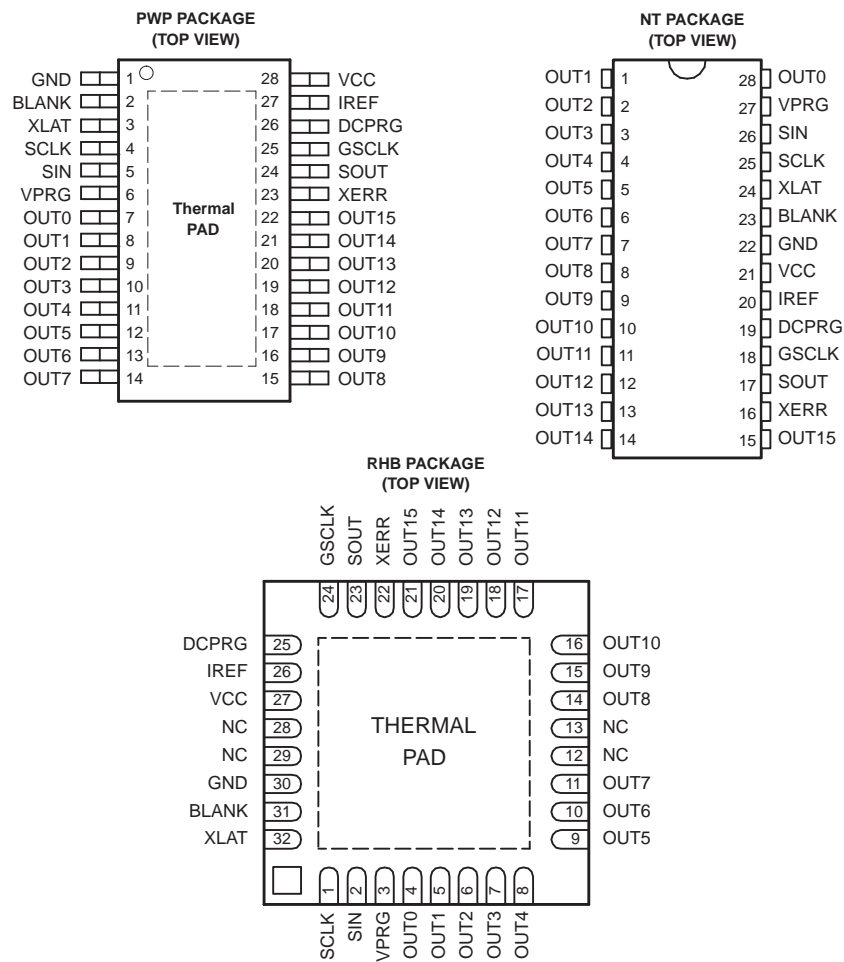
Table 1. Test Parameter Equations

$\Delta(\%) = \frac{I_{OUTn} - I_{OUTavg_0-15}}{I_{OUTavg_0-15}} \times 100$	(1)
$\Delta(\%) = \frac{I_{OUTavg} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \times 100$	(2)
$I_{OUT(IDEAL)} = 31.5 \times \left(\frac{1.24V}{R_{IREF}} \right)$	(3)
$\Delta(\% / V) = \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5V) - (I_{OUTn} \text{ at } V_{CC} = 3.0V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0V)} \times \frac{100}{2.5}$	(4)
$\Delta(\% / V) = \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0V) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1.0V)} \times \frac{100}{2.0}$	(5)

SWITCHING CHARACTERISTICS

$V_{CC} = 3V$ to $5.5V$, $T_A = -40^\circ C$ to $85^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT			16	ns
t_{r1}		OUTn, $V_{CC} = 5V$, $T_A = 60^\circ C$, DCn = 3Fh		10	30	
t_{f0}	Fall time	SOUT			16	ns
t_{f1}		OUTn, $V_{CC} = 5V$, $T_A = 60^\circ C$, DCn = 3Fh		10	30	
t_{pd0}	Propagation delay time	SCLK to SOUT (see Figure 11)			30	ns
t_{pd1}		BLANK to OUT0			60	ns
t_{pd2}		OUTn to XERR (see Figure 11)			1000	ns
t_{pd3}		GSCLK to OUT0 (see Figure 11)			60	ns
t_{pd4}		XLAT to I _{OUT} (dot correction) (see Figure 11)			60	ns
t_{pd5}		DCPRG to OUT0 (see Figure 11)			30	ns
t_d	Output delay time	OUTn to OUT(n+1) (see Figure 11)		20	30	ns
t_{on-err}	Output on-time error	$t_{outon} - T_{gscik}$ (see Figure 11), GS _n = 01h, GSCLK = 11 MHz	10	-50	-90	ns

DEVICE INFORMATION

NC – No internal connection

TERMINAL FUNCTION

NAME	TERMINAL NO.			I/O	DESCRIPTION
	DIP	PWP	RHB		
BLANK	23	2	31	I	Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control.
DCPRG	19	26	25	I	Switch DC data input. When DCPRG = L, DC is connected to EEPROM. When DCPRG = H, DC is connected to the DC register. DCPRG also controls EEPROM writing, when VPRG = V _(PRG) . EEPROM data = 3Fh (default)
GND	22	1	30	G	Ground
GSCLK	18	25	24	I	Reference clock for grayscale PWM control
IREF	20	27	26	I	Reference current terminal
NC	–	–	12, 13, 28, 29		No connection
OUT0	28	7	4	O	Constant current output
OUT1	1	8	5	O	Constant current output
OUT2	2	9	6	O	Constant current output
OUT3	3	10	7	O	Constant current output
OUT4	4	11	8	O	Constant current output
OUT5	5	12	9	O	Constant current output
OUT6	6	13	10	O	Constant current output
OUT7	7	14	11	O	Constant current output
OUT8	8	15	14	O	Constant current output
OUT9	9	16	15	O	Constant current output
OUT10	10	17	16	O	Constant current output
OUT11	11	18	17	O	Constant current output
OUT12	12	19	18	O	Constant current output
OUT13	13	20	19	O	Constant current output
OUT14	14	21	20	O	Constant current output
OUT15	15	22	21	O	Constant current output
SCLK	25	4	1	I	Serial data shift clock
SIN	26	5	2	I	Serial data input
SOUT	17	24	23	O	Serial data output
VCC	21	28	27	I	Power supply voltage
VPRG	27	6	3	I	Multifunction input pin. When VPRG = GND, the device is in GS mode. When VPRG = V _{CC} , the device is in DC mode. When VPRG = V _(VPRG) , DC register data can be programmed into DC EEPROM with DCPRG=HIGH. EEPROM data = 3Fh (default)
XERR	16	23	22	O	Error output. XERR is an open-drain terminal. XERR goes L when LOD or TEF is detected.
XLAT	24	3	32	I	Level triggered latch signal. When XLAT = high, the TLC5940 writes data from the input shift register to either GS register (VPRG = low) or DC register (VPRG = high). When XLAT = low, the data in GS or DC register is held constant.

PARAMETER MEASUREMENT INFORMATION**PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**

Resistor values are equivalent resistances, and they are not tested.

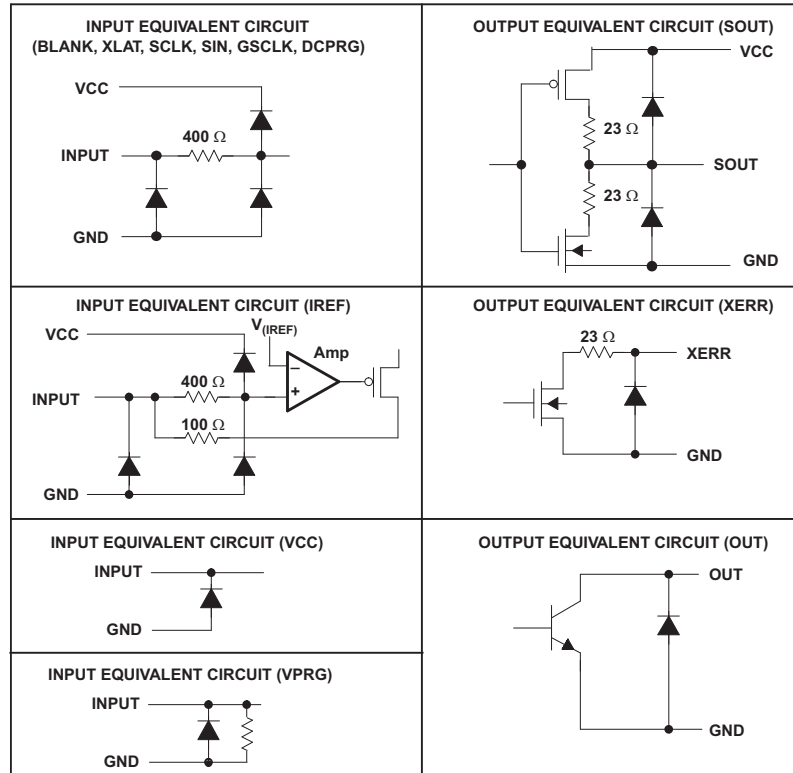


Figure 1. Input and Output Equivalent Circuits

PARAMETER MEASUREMENT INFORMATION (continued)

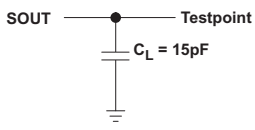
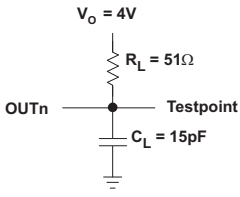
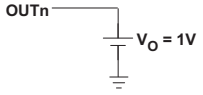
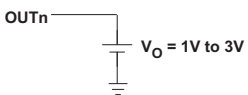
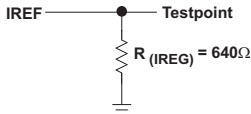
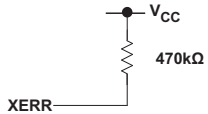
t_{r0}, t_{f0}, t_{pd0} 	$t_{r1}, t_{f1}, t_{pd1}, t_{pd2}, t_{pd3}, t_{pd4}, t_{pd5}, t_d$ 
$I_{O(LC)}, \Delta I_{O(LC0)}, \Delta I_{O(LC1)}, \Delta I_{O(LC2)}, \Delta I_{O(LC3)}$ 	$\Delta I_{O(LC4)}$ 
$V_{(IREF)}$ 	t_{pd3} 

Figure 2. Parameter Measurement Circuits

TYPICAL CHARACTERISTICS

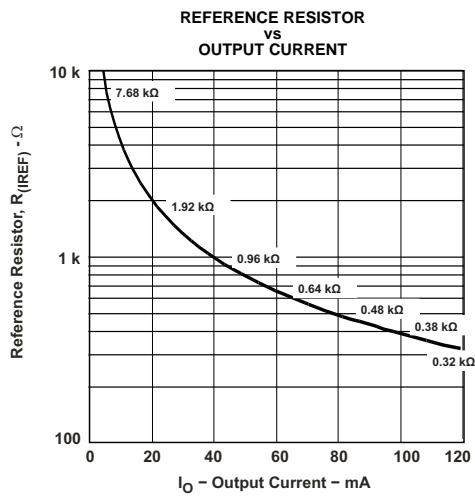


Figure 3.

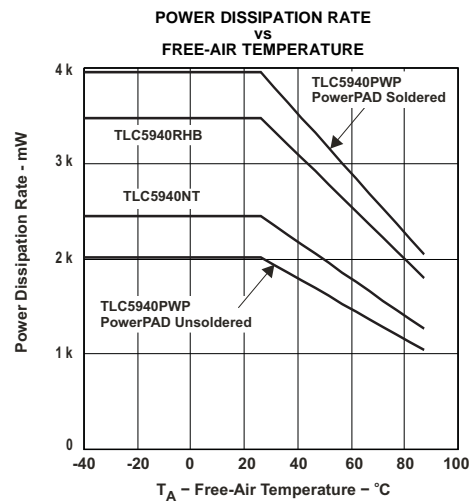


Figure 4.

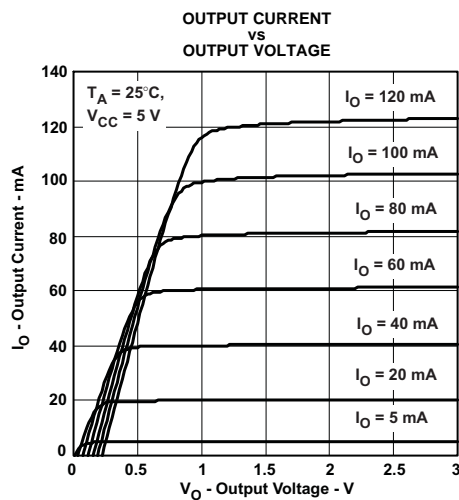


Figure 5.

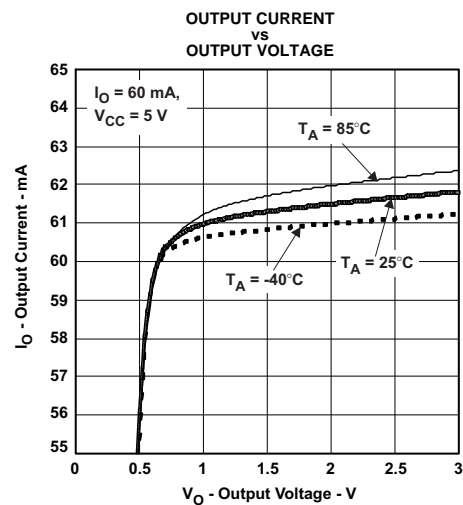


Figure 6.

TYPICAL CHARACTERISTICS (continued)

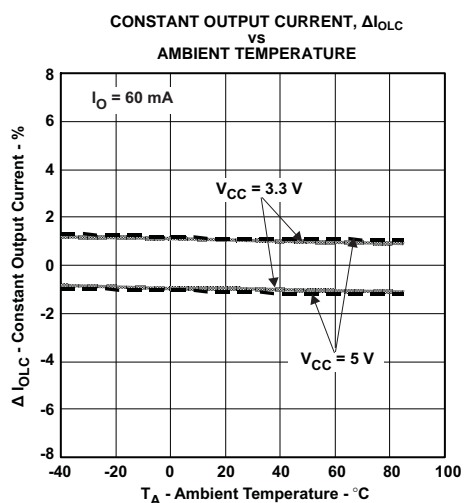


Figure 7.

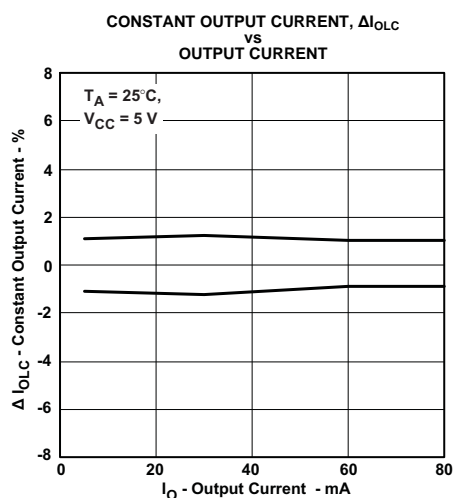


Figure 8.

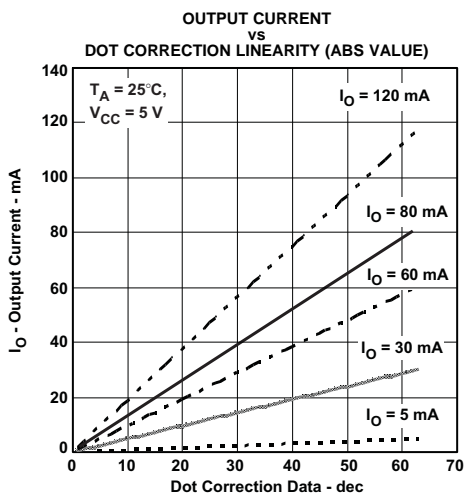


Figure 9.

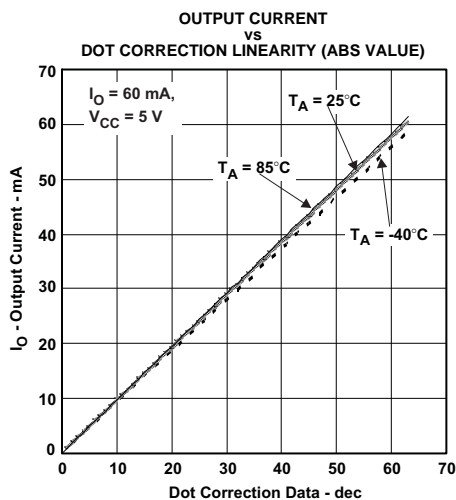


Figure 10.

PRINCIPLES OF OPERATION

SERIAL INTERFACE

The TLC5940 has a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only 3 pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data is clocked in, a high-level pulse of XLAT signal latches the serial data to the internal registers. The internal registers are level-triggered latches of XLAT signal. All data are clocked in with the MSB first. The length of serial data is 96 bit or 192 bit, depending on the programming mode. Grayscale data and dot correction data can be entered during a grayscale cycle. Although new grayscale data can be clocked in during a grayscale cycle, the XLAT signal should only latch the grayscale data at the end of the grayscale cycle. Latching in new grayscale data immediately overwrites the existing grayscale data. Figure 11 shows the timing chart. More than two TLC5940s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. An example of cascading two TLC5940s is shown in Figure 12 and the timing chart is shown in Figure 13. The SOUT pin can also be connected to the controller to receive status information from TLC5940 as shown in Figure 22.

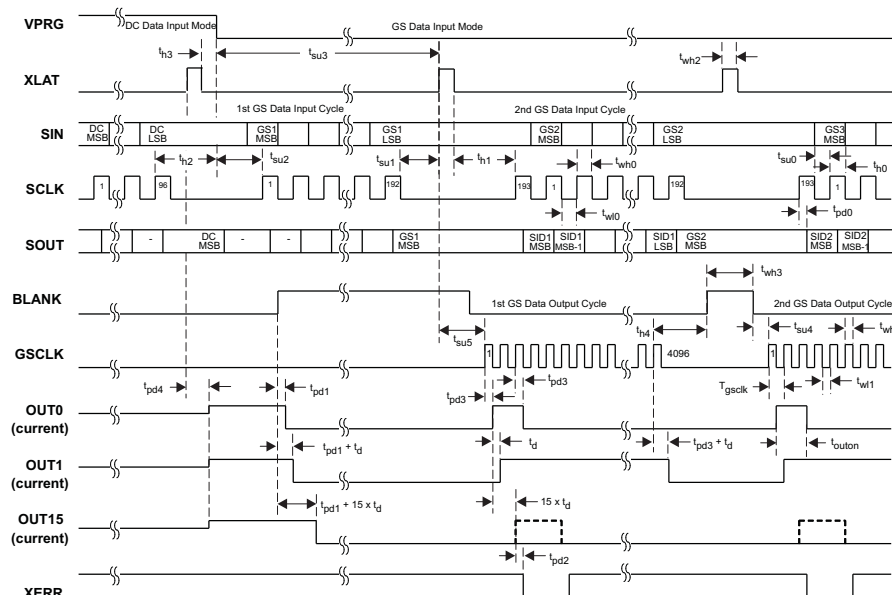


Figure 11. Serial Data Input Timing Chart

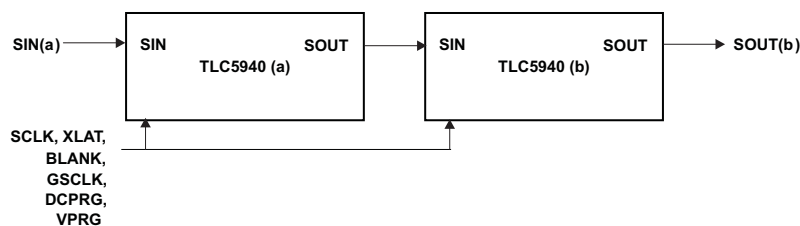


Figure 12. Cascading Two TLC5940 Devices

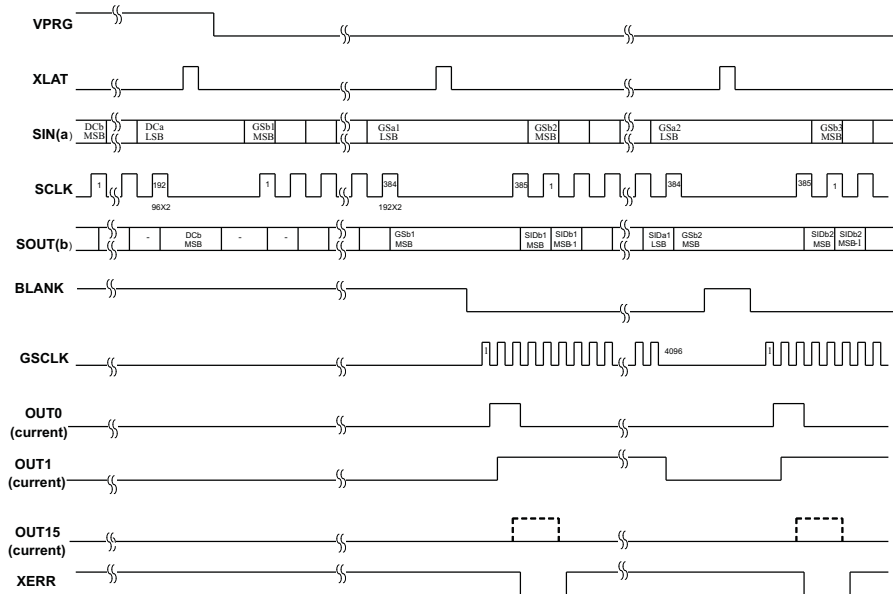


Figure 13. Timing Chart for Two Cascaded TLC5940 Devices

ERROR INFORMATION OUTPUT

The open-drain output XERR is used to report both of the TLC5940 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Since XERR is an open-drain output, multiple ICs can be OR'ed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error (see Figure 22).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 2. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	$OUTn > V_{(LED)}$	L	L	L	H
	$OUTn < V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	$OUTn > V_{(LED)}$	H	L		L
	$OUTn < V_{(LED)}$	H	H		L

TEF: THERMAL ERROR FLAG

The TLC5940 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160°C typical), TEF becomes H and XERR pin goes to low level. When the junction temperature becomes lower than the threshold temperature, TEF becomes L and XERR pin becomes high impedance. TEF status can also be read out from the TLC5940 status register.

LOD: LED OPEN DETECTION

The TLC5940 has an LED-open detector that detects broken or disconnected LEDs. The LED open detector pulls the XERR pin to GND when an open LED is detected. XERR and the corresponding error bit in the Status Information Data is only active under the following open-LED conditions.

1. OUTn is on and the time tpd2 (1 μ s typical) has passed.
2. The voltage of OUTn is < 0.3V (typical)

The LOD status of each output can be also read out from the SOUT pin. See STATUS INFORMATION OUTPUT section for details. The LOD error bits are latched into the Status Information Data when XLAT returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

DELAY BETWEEN OUTPUTS

The TLC5940 has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see the functional block diagram). The fixed-delay time is 20ns (typical), OUT0 has no delay, OUT1 has 20ns delay, and OUT2 has 40ns delay, etc. The maximum delay is 300ns from OUT0 to OUT15. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

OUTPUT ENABLE

All OUTn channels of the TLC5940 can be switched off with one signal. When BLANK is set high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set low, all OUTn channels work under normal conditions. If BLANK goes low and then back high again in less than 300ns, all outputs programmed to turn on still turn on for either the programmed number of grayscale clocks, or the length of time that the BLANK signal was low, whichever is lower. For example, if all outputs are programmed to turn on for 1ms, but the BLANK signal is only low for 200ns, all outputs still turn on for 200ns, even though some outputs are turning on after the BLANK signal has already gone high.

Table 3. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

SETTING MAXIMUM CHANNEL CURRENT

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current per channel can be calculated by Equation 6:

$$I_{max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5 \quad (6)$$

where:

$$V_{(IREF)} = 1.24 \text{ V}$$

$$R_{(IREF)} = \text{User-selected external resistor.}$$

I_{max} must be set between 5 mA and 120 mA. The output current may be unstable if I_{max} is set lower than 5 mA. Output currents lower than 5 mA can be achieved by setting I_{max} to 5 mA or higher and then using dot correction.

Figure 3 shows the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 31.5 times the current flowing out of the IREF pin.

POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rating of the device package to ensure correct operation. Equation 7 calculates the power dissipation of device:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{MAX} \times \frac{DC_n}{63} \times d_{PWM} \times N) \quad (7)$$

where:

- V_{CC} : device supply voltage
- I_{CC} : device supply current
- V_{OUT} : TLC5940 OUTn voltage when driving LED current
- I_{MAX} : LED current adjusted by $R_{(REF)}$ Resistor
- DC_n : maximum dot correction value for OUTn
- N : number of OUTn driving LED at the same time
- d_{PWM} : duty cycle defined by BLANK pin or GS PWM value

OPERATING MODES

The TLC5940 has operating modes depending on the signals DCPRG and VPRG. Table 4 shows the available operating modes. The TPS5940 GS operating mode (see Figure 11) and shift register values are not defined after power up. One solution to solve this is to set dot correction data after TLS5940 power-up and switch back to GS PWM mode. The other solution is to overflow the input shift register with 193 bits of dummy data and latch it while TLS540 is in GS PWM mode. The values in the input shift register, DC register and GS register are unknown just after power on. The DC and GS register values should be properly stored through the serial interface before starting the operation.

Table 4. TLC5940 Operating Modes Truth Table

SIGNAL		INPUT SHIFT REGISTER	MODE	DC VALUE
DCPRG	VPRG			
L	GND	192 bit	Grayscale PWM Mode	EEPROM
H				DC Register
L	V_{CC}	96 bit	Dot Correction Data Input Mode	EEPROM
H				DC Register
L	$V_{(VPRG)}$	X	EEPROM Programming Mode	EEPROM
H				Write dc register value to EEPROM. (Default data: 3Fh)

SETTING DOT CORRECTION

The TLC5940 has the capability to fine adjust the output current of each channel OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max} . Dot correction for all channels must be entered at the same time. Equation 8 determines the output current for each output n:

$$I_{OUTn} = I_{max} \times \frac{DC_n}{63} \quad (8)$$

where:

- I_{max} = the maximum programmable output current for each output.
- DC_n = the programmed dot correction value for output n ($DC_n = 0$ to 63).
- $n = 0$ to 15

Figure 14 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc. The DC 15.5 in Figure 14 stands for the 5th most significant bit for output 15.

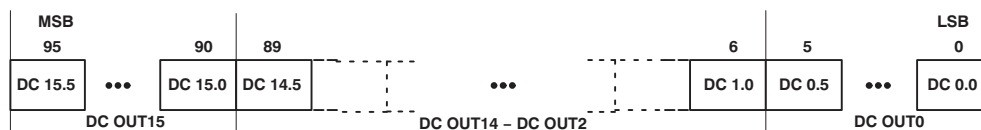


Figure 14. Dot Correction Data Packet Format

When VPRG is set to VCC, the TLC5940 enters the dot correction data input mode. The length of input shift register becomes 96 bits. After all serial data are shifted in, the TLC5940 writes the data in the input shift register to DC register when XLAT is high, and holds the data in the DC register when XLAT is low. The DC register is a level triggered latch of XLAT signal. Since XLAT is a level-triggered signal, SCLK and SIN must not be changed while XLAT is high. After XLAT goes low, data in the DC register is latched and does not change. BLANK signal does not need to be high to latch in new data. XLAT has setup time (t_{su1}) and hold time (t_{h1}) to SCLK as shown in Figure 15.

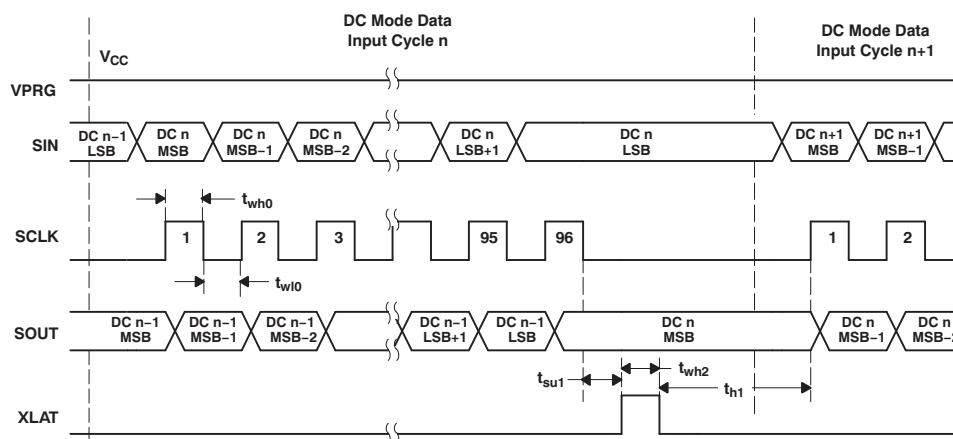


Figure 15. Dot Correction Data Input Timing Chart

The TLC5940 also has an EEPROM to store dot correction data. To store data from the dot correction register to EEPROM, DCPRG is set to high after applying V_{PRG} to the VPRG pin. Figure 16 shows the EEPROM programming timings. The EEPROM has a default value of all 1s.

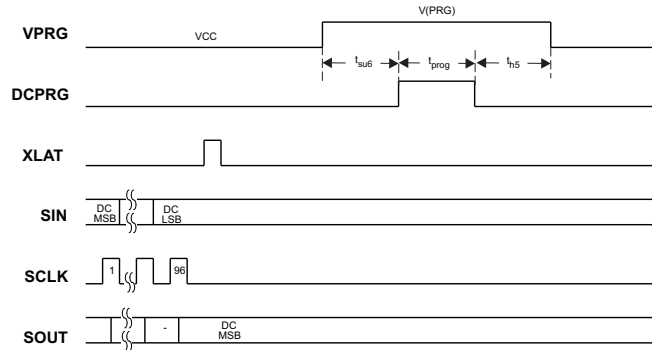


Figure 16. EEPROM Programming Timing Chart

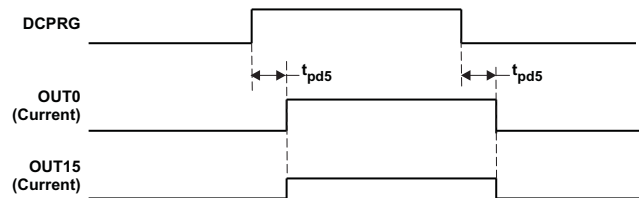


Figure 17. DCPRG and OUTn Timing Diagram

SETTING GRAYSCALE

The TLC5940 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, respective 0% to 100% brightness. Equation 9 determines the brightness level for each output n:

$$\text{Brightness in \%} = \frac{\text{GS}_n}{4095} \times 100 \quad (9)$$

where:

GS_n = the programmed grayscale value for output n (GS_n = 0 to 4095)

n = 0 to 15

Grayscale data for all OUTn

Figure 18 shows the grayscale data packet format which consists of 12 bits x 16 channels, totaling 192 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc.



Figure 18. Grayscale Data Packet Format

When VPRG is set to GND, the TLC5940 enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the XLAT signal latches the data into

the grayscale register (see Figure 11). New grayscale data immediately becomes valid at the rising edge of the XLAT signal; therefore, new grayscale data should be latched at the end of a grayscale cycle when BLANK is high. The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after updated the grayscale register.

STATUS INFORMATION OUTPUT

The TLC5940 does have a status information register, which can be accessed in grayscale mode (VPRG=GND). After the XLAT signal latches the data into the GS register the input shift register data will be replaced with status information data (SID) of the device (see Figure 18). LOD, TEF, and dot correction EEPROM data (DCPRG=LOW) or dot correction register data (DCPRG=HIGH) can be read out at SOUT pin. The status information data packet is 192 bits wide. Bits 0-15 contain the LOD status of each channel. Bit 16 contains the TEF status. If DCPRG is low, bits 24-119 contain the data of the dot-correction EEPROM. If DCPRG is high, bits 24-119 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 19.

SOUT outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown Figure 20. The next SCLK pulse, which will be the clock for receiving the SMB of the next grayscale data, transmits MSB-1 of SID. If output voltage is < 0.3 V (typical) when the output sink current turns on, LOD status flag becomes active. The LOD status flag is an internal signal that pulls XERR pin down to low when the LOD status flag becomes active. The delay time, tpd2 (1 μ s maximum), is from the time of turning on the output sink current to the time LOD status flag becomes valid. The timing for each channel's LOD status to become valid is shifted by the 30-ns (maximum) channel-to-channel turn-on time. After the first GSCLK goes high, OUT0 LOD status is valid; tpd3 + tpd2 = 60 ns + 1 μ s. OUT1 LOD status is valid; tpd3 + td + tpd2 = 60 ns + 30 ns + 1 μ s = 1.09 μ s. OUT2 LOD status is valid; tpd3 + 2*td + tpd2 = 1.12 μ s, and so on. It takes 1.51 μ s maximum (tpd3 + 15*td + tpd2) from the first GSCLK rising edge until all LOD become valid; *tsuLOD* must be > 1.51 μ s (see Figure 20) to ensure that all LOD data are valid.

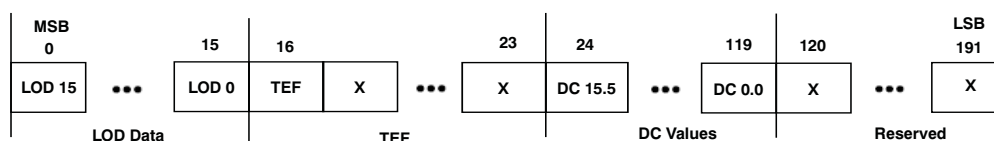


Figure 19. Status Information Data Packet Format

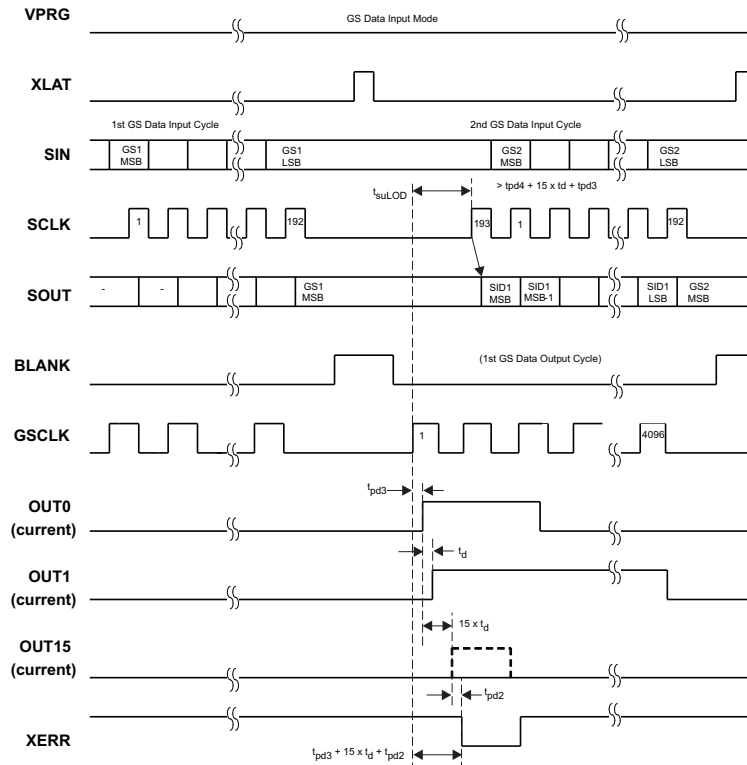


Figure 20. Readout Status Information Data (SID) Timing Chart

GRAYSCALE PWM OPERATION

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK goes low increases the grayscale counter by one and switches on all OUTn with grayscale value not zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC5940 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to the counter values are switched off. A BLANK=H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 21). When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling BLANK high before the counter reaches FFFh immediately resets the counter to zero.

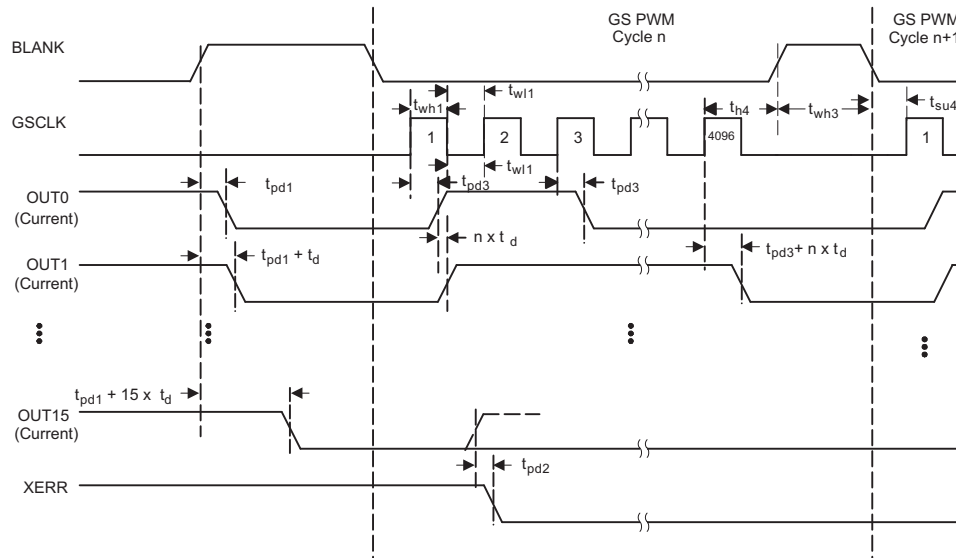


Figure 21. Grayscale PWM Cycle Timing Chart

SERIAL DATA TRANSFER RATE

Figure 22 shows a cascading connection of n TLC5940 devices connected to a controller, building a basic module of an LED display system. The maximum number of cascading TLC5940 devices depends on the application system and is in the range of 40 devices. Equation 10 calculates the minimum frequency needed:

$$f_{\text{(GSCLK)}} = 4096 \times f_{\text{(update)}}$$

$$f_{\text{(SCLK)}} = 193 \times f_{\text{(update)}} \times n \quad (10)$$

where:

- $f_{\text{(GSCLK)}}$: minimum frequency needed for GSCLK
- $f_{\text{(SCLK)}}$: minimum frequency needed for SCLK and SIN
- $f_{\text{(update)}}$: update rate of whole cascading system
- n : number cascaded of TLC5940 device

APPLICATION EXAMPLE

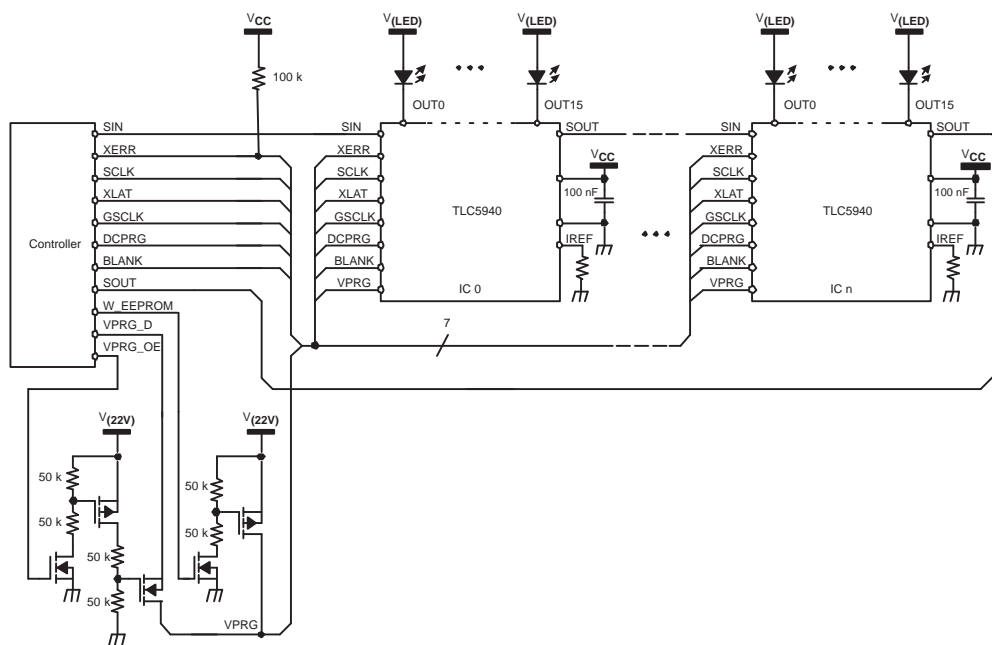


Figure 22. Cascading Devices

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC5940NT	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
TLC5940NTG4	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
TLC5940PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5940PWPG4	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5940PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5940PWPRG4	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5940RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5940RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

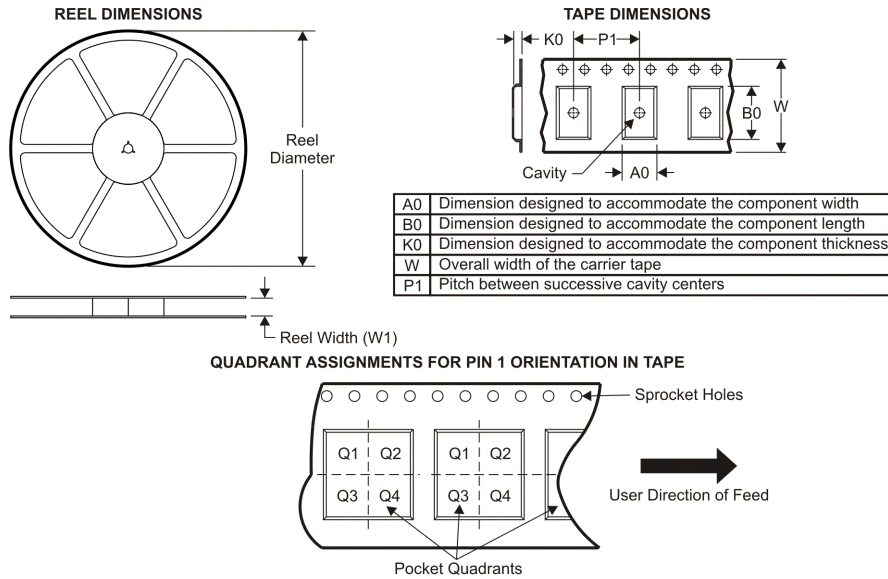
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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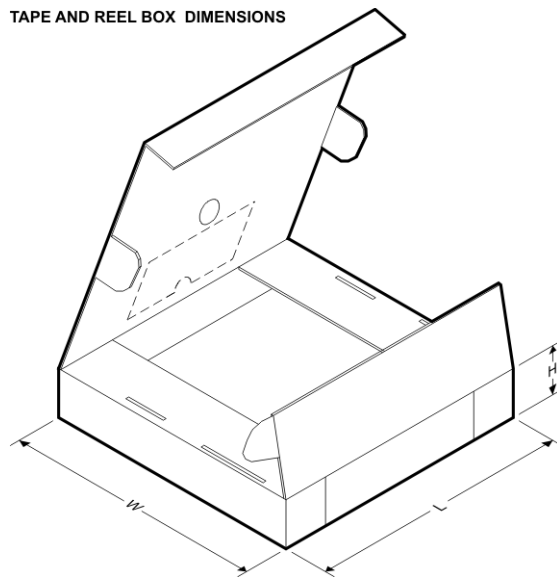
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5940PWPR	HTSSOP	PWP	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1
TLC5940RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

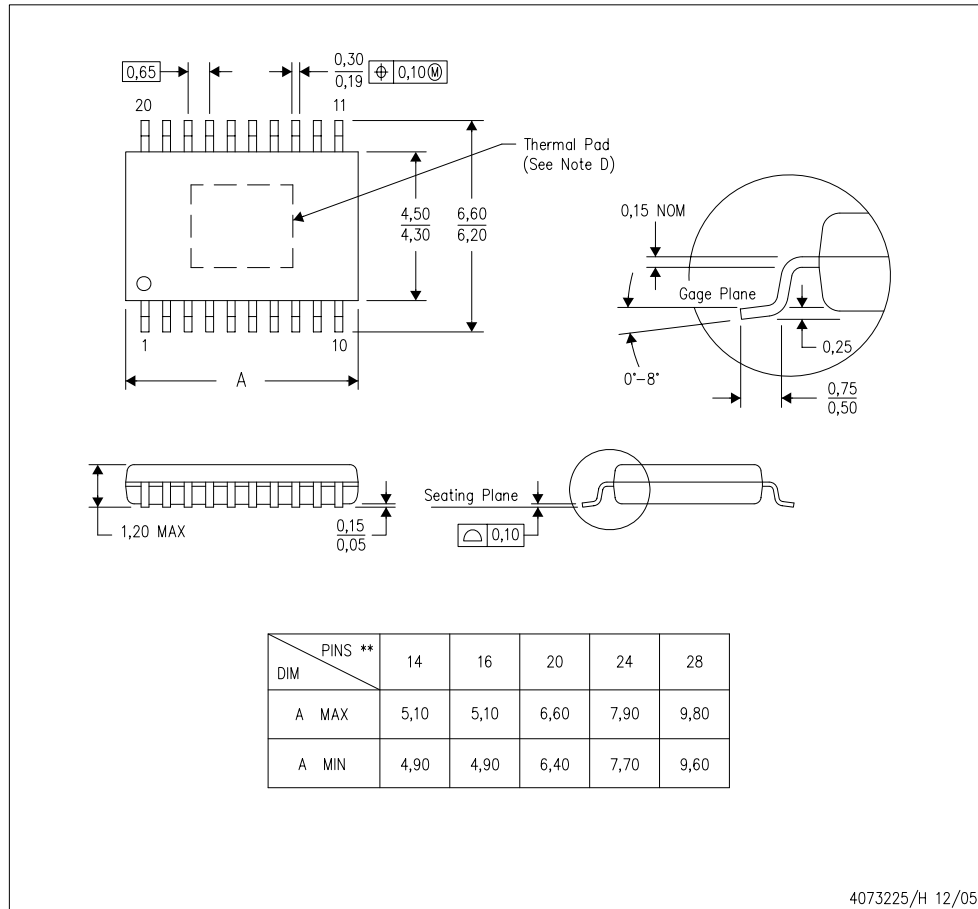


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5940PWPR	HTSSOP	PWP	28	2000	346.0	346.0	33.0
TLC5940RHBR	QFN	RHB	32	3000	346.0	346.0	29.0

MECHANICAL DATA

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE
20 PIN SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0,15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-153

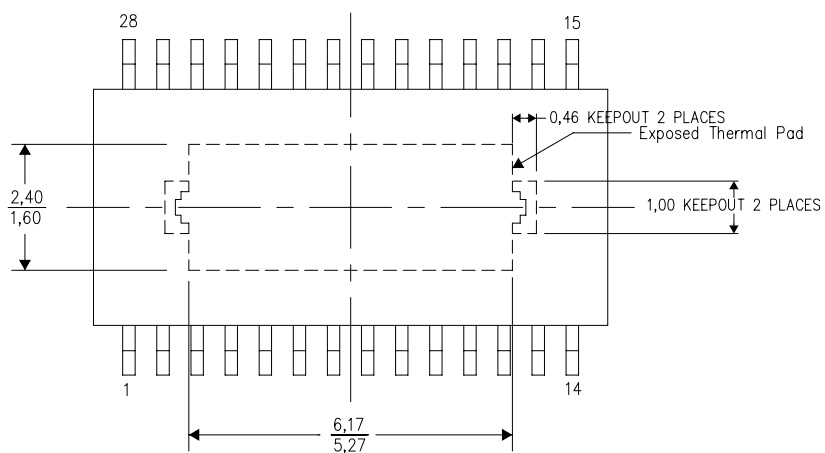
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

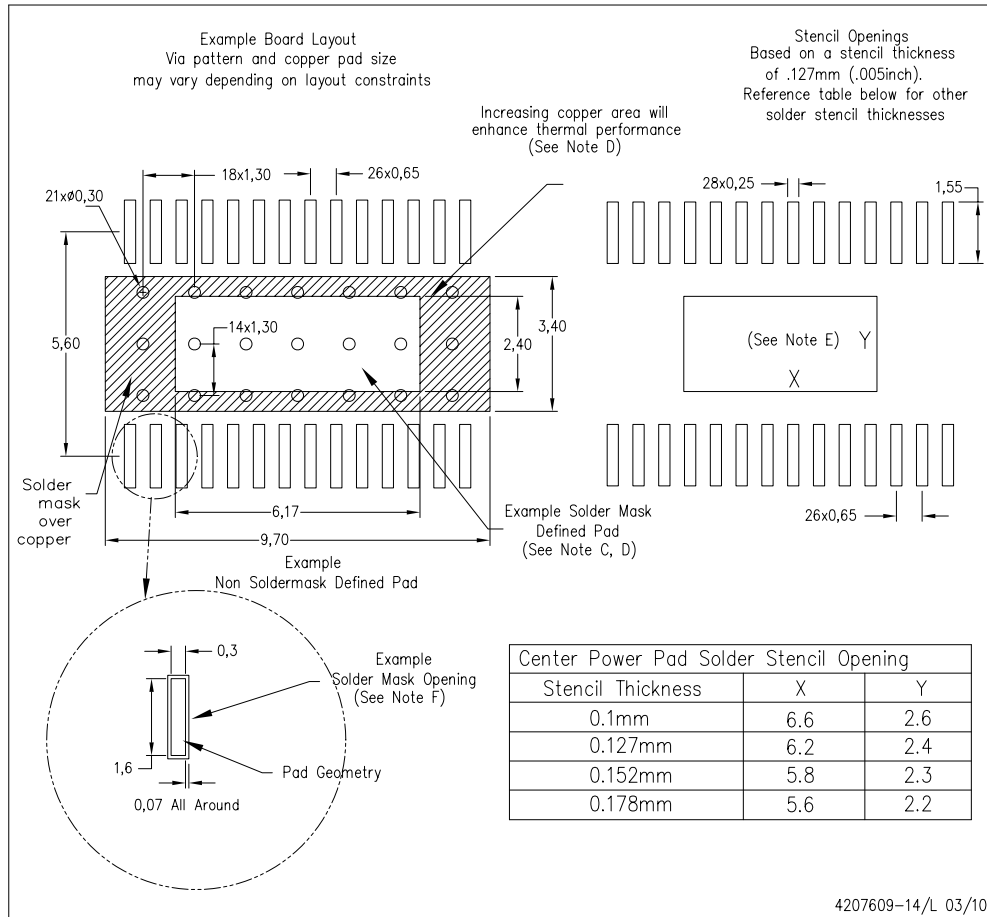


Exposed Thermal Pad Dimensions

LAND PATTERN

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

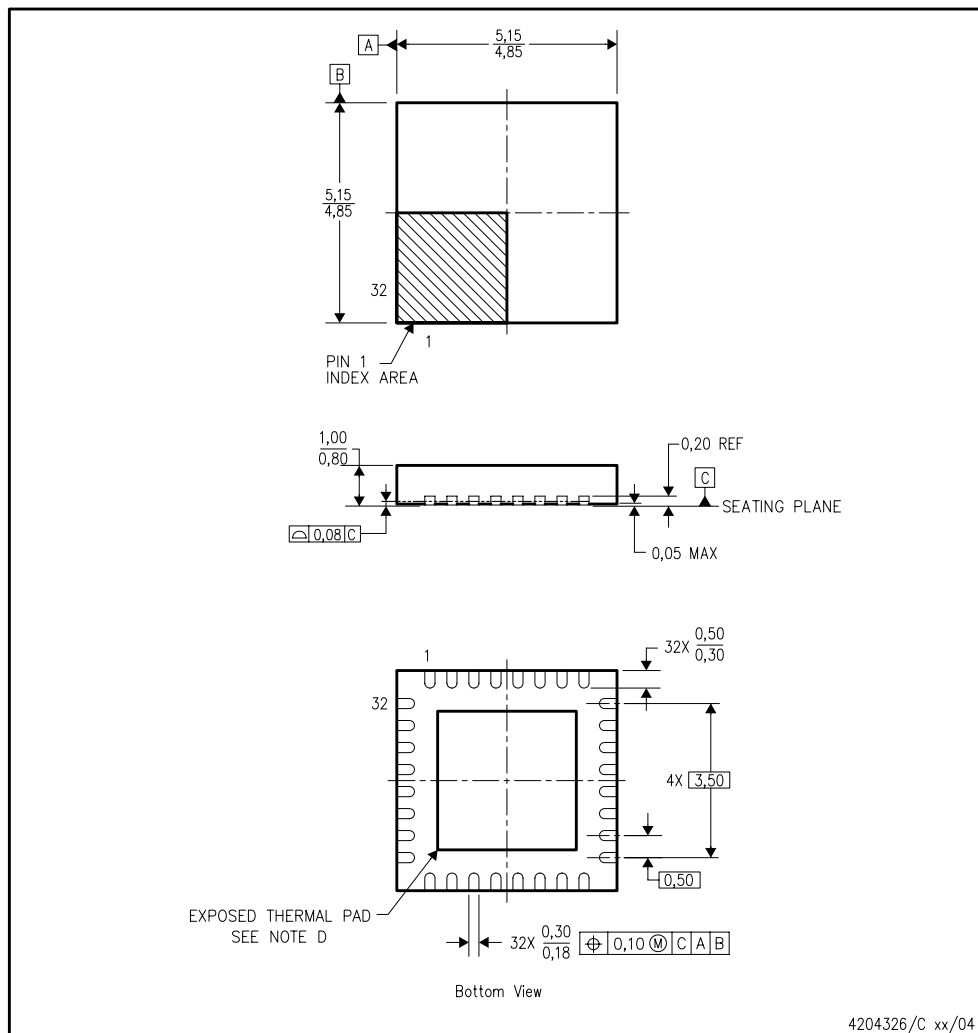
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
- For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

MECHANICAL DATA

RHB (S-PQFP-N32)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RHB (S-PVQFN-N32)

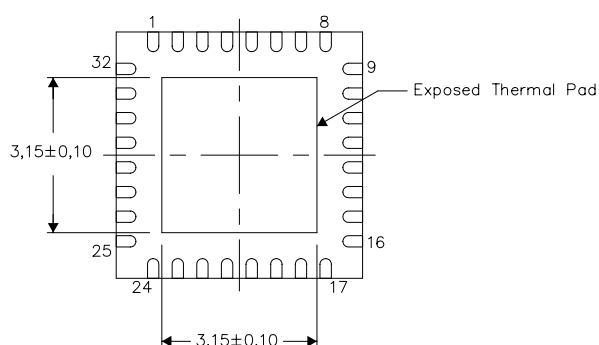
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

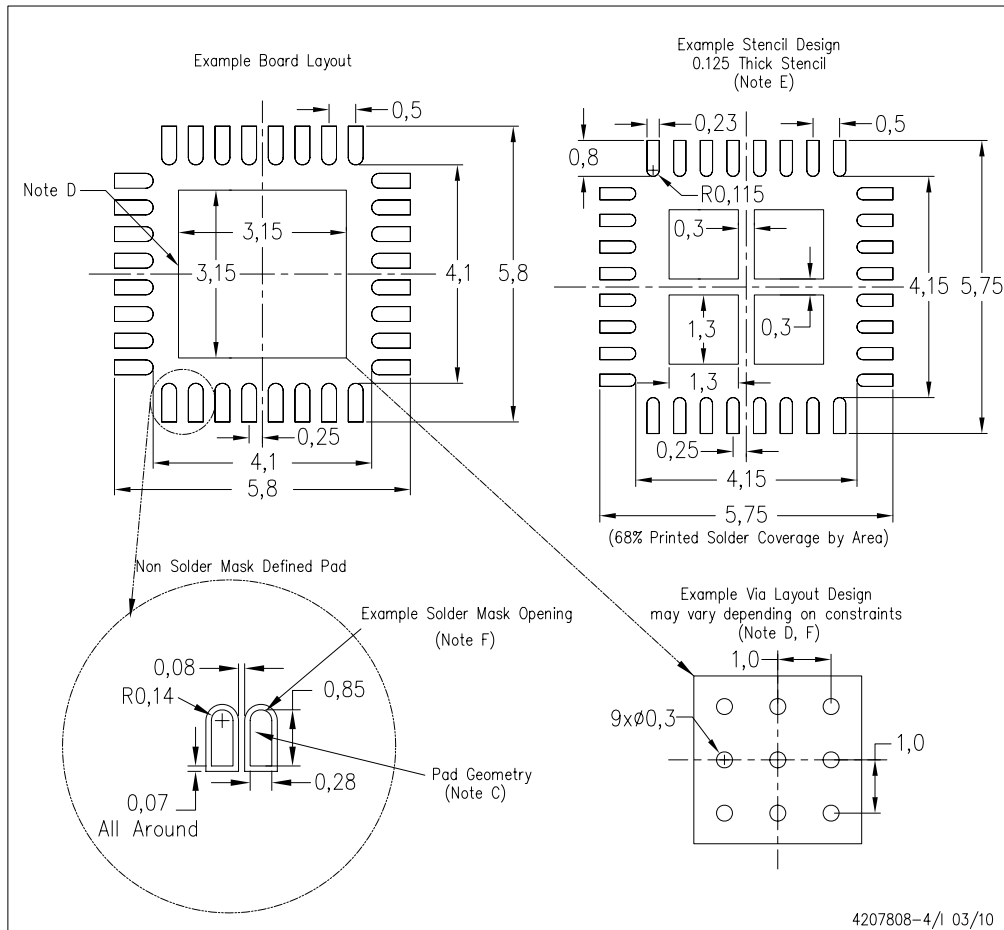
Exposed Thermal Pad Dimensions

4206356-4/0 06/10

LAND PATTERN

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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