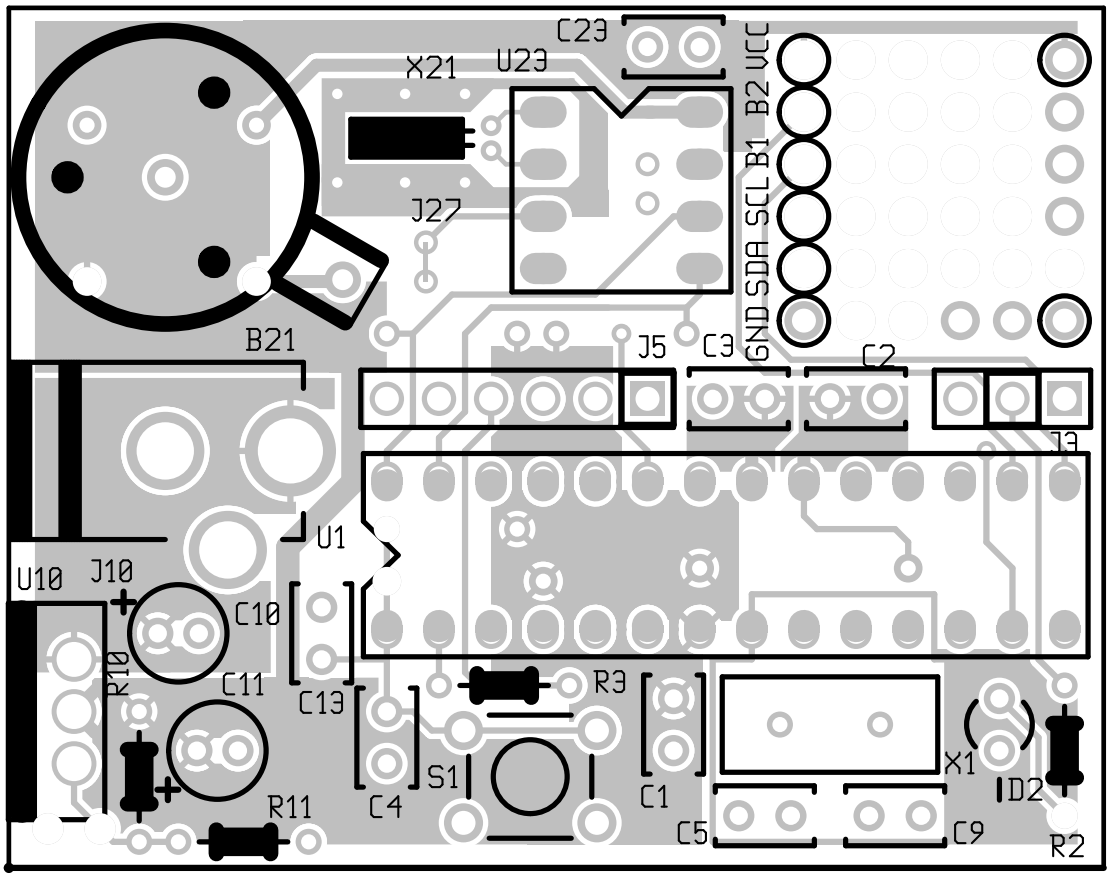

PICO1TRC Description

The PICO1TRC is a low-cost microcontroller development board that is compatible with the Arduino development tools. The board is 2.1" x 1.65" and all the I/O pins from the ATmega328 are brought out on 2 rows of 14 pins (300mil spacing).

Features

- **2.1" x 1.65"**
- Replaceable and upgradeable CPU
- Compatible with the Arduino development tools.
- ATmega328P running at 12MHz
- Adjustable Linear Regulator (V_{cc} = 3.3V to 5V) Output voltage is set by changing one resistor. Resistors for 3.3V and 5V operation are included.
- 0.6" x 0.6" prototyping area
- Two rows of 14 pins (300mil spacing) with all ATmega328 I/O functions.
- Six pin header for FTDI TTL-232R-3V3 cable.
- Debug LED that can be jumpered to Pin 7 or disconnected.
- A/D reference supply filtered per Atmel specification.
- Reset circuit per Atmel specification.

1 Assembling the PICO1TRC

Semiconductors are electrostatic-sensitive devices. Proper ESD handling precautions need to be taken to avoid damage.

Do not cut any of the U1 socket pins until you have determined which pins are needed in your application. All of the PICO1TRC I/O pins are the U1 socket pins. See subsection 1.7 for pin removal information.

The Bill of Materials (BOM) and Component List are in section 6. For full page assembly drawings see Figure 1 (top) and Figure 2 (bottom).

The kit includes resistors to trim the output regulator to 3.3V or 5V. When you are done assembling the kit you will have one extra resistor. If you have build a 3.3V board you will have a 1KΩ resistor left. If you have built a 5V board you will have either a 205 or 210Ω resistor left.

1.1 Bottom Side Components

- D1

  Line the cathode marking on D1 with the cathode marking on the silkscreen

- D21, D22

  Line the cathode marking of D21,D22 with the cathode marking on the silkscreen

- L1

  The value of inductor L1 is not critical. Kits will contain an inductor with a value between 10µH and 20µH

- R1, R22, R23

  10KΩ *(brown, black, black, red, brown)*

- C12 (optional, not included)

  C12 is a noise reduction capacitor for the LDO regulator (U4). It is not required for most applications and is not included in the kit. The suggested value in the manufacturer's datasheet is 0.1µF.

1.2 Real-time Clock Circuit Assembly

- X21 crystal
- U23 socket
- B21 battery holder
- C23

1.3 Power Supply Circuit Assembly

Solder the top side components:

- C10, C11

  C10 and C11 are polarized parts. The long lead is the positive. The short lead is the negative. Make sure that the **positive** *lead is inserted into positive hole in the PCB*

- R10

  124Ω *(brown, red, yellow, black, brown)*

- R11

  For 3.3V operation this value will be either 205Ω (red, black, green, black, brown) or 210Ω (red, brown, black, black, brown) For 5V operation this value will be 374Ω (orange, violet, yellow, black, brown)

- U10

  Make sure that the tab is aligned to the tab marking on the PCB.

- J10

1.4 Microcontroller Circuit Assembly

Solder the top side components:

- C1, C2, C3, C13, C4 (optional).

  C4 is optional and is not included in the kit. It is meant for applications that require additional filtering of the reset line. The reset function that uses the /RTS line from the USB interface will not function with C4 installed.

- D2

  The negative lead of the LED is the short lead. Align the short lead with the negative marking on the PCB.

- R2

  For 3.3V operation use the 374Ω (orange, violet, yellow, black, brown). For 5V operation use the 1KΩ (brown, black, black brown, brown)

- R3

  *10*KΩ *(brown, black, black, red, brown)*

- J3
- J5
- X1, C5, C9
- U1 (socket)

1.5 Electro-mechanical Components

Since the reset switch (S1) is sensitive to washing it should be placed on last. Lightly clean the board after the switch is installed. If water does get into the switch let it dry out before applying power.
Solder the top side components:

- S1

1.6 IC Installation and Test

1.6.1 U23 (DS1337)

Remove the DS1337 from the antistatic foam and insert it into the socket aligning the notch in the IC package with the notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

1.6.2 U1 (ATmega328P)

Remove the ATmega328P from the antistatic foam and insert it into the socket aligning the notch in the IC package with the notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

1.6.3 B21 (CR1220 coin cell)

Install a CR1220 coin cell into the battery holder (`B21`) observing the polarity indicated on the holder.

The PICO1TRC should now be fully functional and is ready to program (see section 5). Depending on the application some of the pins on the `U1` socket should be removed (see subsection 1.7).

1.7 Pin Removal

After operation of the PICO1TRC is verified it is recommended that some of the U1 pins be cut flush to the PCB level. Each application is different and needs to reviewed. Pins like `XTAL1` and `XTAL2` can be affected by stray capacitance and noise. For most applications cutting the `XTAL1`, `XTAL2`, `AREF` and `AVCC` is recommended.

If your application may change over time then leave all pins intact and use care in your layout.

1.7.1 XTAL Pins

The XTAL circuit is susceptible to stray capacitance and noise so pins 9 and 10 should be cut flush to the PCB.

1.7.2 AREF

If you are not using an external analog reference then cut pin 21 flush to the board.

1.7.3 AVCC

If you are not powering the ADC from a different source then pin 20 should be cut flush to the board.

2 IO Connectors

J5 USB header for an FTDI TTL-232R-3V3 cable.

J10 Input power jack. See subsection 3.1

3 Electrical Hints

3.1 Power Supply

The PICO1TRC is powered by a DC output wall adapter with an output voltage from 5.3V to 18V. The input voltage is limited by the amount of power dissipated in the linear regulator (`U4`). This varies by application.

It is critcal to keep the power dissipation in the LDO regulator (U4), to less than one watt. The voltage drop across U4 is

$$V_{drop} = V_{in} - V_{out}$$

Where V_{in} is the input voltage connected to `J10` and V_{out} is the output voltage (see subsection 3.2). The power dissipated in U4 is given by

$$P_{diss} = V_{drop} \cdot I_{system}$$

where I_{system} is the load of the PICO1TRC plus its peripheral circuitry.

3.2 Changing V_{cc}

V_{cc}, which is the output of the MC33269T regulator, is adjusted by changing the value of `R11`. The equation for V_{cc} is –

$$V_{cc} = 1.24 \cdot \frac{124 + R_{11}}{124}$$

R_{11} values for common output voltages are listed in Table 1. The PICO1TRC kits come with both values listed in the table.

R_2 adjusts the current through the debug LED. At a forward current (I_f) of 2mA the LED has a typical forward voltage (V_f) of 2V. An I_f between 2mA and 5mA provides a reasonable brightness. The equation for R_2 is

$$\frac{V_{CC} - 2\text{V}}{5\text{mA}} < R_2 < \frac{V_{CC} - 2\text{V}}{2\text{mA}}$$

Recommended R_2 values are shown in Table 1.

V_{cc} (volts)	R_{11} (ohms)	R_2 (ohms)
3.3	205	374
5.0	374	1000

Table 1: R_{11} and R_2 values for 3.3V and 5V Operation

4 Real-Time Clock

The PICO1TRC real-time clock (RTC) consists of a DS1337 that is powered by a CR1220 coin cell or the PICO1TRC linear regulator (U10). The or'ing diodes, D21 and D22, will output the higher voltage to the RTC (U23).

Communication to the DS1337 is through the I²C interface (a.k.a. two-wire or TWI). The I²C pullup resistors are on board (10KΩ). The interrupt lines, `/INTA` and `/INTB` are jumpered to PC3 (Arduino pin 17) and PC0 (Arduino pin 14) respectively. There are no pullup resistors on the interrupt lines. If external pullups are not added then the internal pullups of the ATmega328P need to be used.

Programming the RTC requires a software library for the DS1337 and for the TWI interface. Both of these libraries are on the wiblocks site.

4.1 I²C Pullup Resistors

The maximum bus capacitance of the I²C bus is 400pF. Unless a large number of devices are on the bus or devices are connected using long cables PICO1TRC system will not get close to this limit. The DS1337 represents a maximum load of 10pF.

The minimum pullup resistance is 966Ω ($\frac{V_{CC}-0.4V}{3mA}$). The maximum value pullup resistance is

$$R_{pullup(max)} = \begin{cases} \frac{1000nS}{C_{BUS}} & \text{if } F_{SCL} \leq 100kHz, \\ \frac{300nS}{C_{BUS}} & \text{if } 100kHz < F_{SCL} \leq 400kHz. \end{cases}$$

where C_{BUS} is the maximum bus capacitance, , and V_{CC} is 3.3V for the PICO1TRC.

With a 100pF load (10 times the DS1337 load), the maximum resistance for 400kHz operation is 3KΩ. For 100kHz the maximum resistance is 10KΩ. If only the DS1337 is on the I²C bus the maximum resistances would be 100KΩ (100kHz) and 30KΩ (400kHz). The minimum resistance, which is not dependent on bus capacitance, is 966Ω for any operating frequency and C_{BUS}. (Atmel, 2009a)

CBUS	**100**pF		**400**pF	
Frequency	**Resistance**		**Resistance**	
	Min	**Max**	**Min**	**Max**
100kHz	1150Ω	10KΩ	1150Ω	2500Ω
400kHz	1150Ω	3KΩ	–Not Practical–	

Table 2: I²C Pullup Resistors

4.2 DS1337 Interrupt Lines

The DS1337 interrupt lines, `/INTA` and `/INTB` are jumpered to PC3 (Arduino pin 17) and PC0 (Arduino pin 14) respectively. To disconnect `/INTA` cut jumper `J24`. To disconnect `/INTB` cut jumper `J27`.

There are no pullup resistors connected to the interrupt lines. To use the interrupt lines with the ATmega328P the internal pull-up resistors need to be enabled. For the ATmega328P 20KΩ ≤ R_{pullup} ≤ 50KΩ which is sufficient to pullup the DS1337 lines. (Atmel, 2009b).

4.3 RTC Battery Life

The DS1337 operates with a V_{CC} from 1.8V to 5.5V. When power is removed from the PICO1TRC the DS1337 is in standby mode and the maximum standby current is 1.5μA(Maxim, 2009a). The CR1220 coin cell has a capacity of 40mAH (to 2V). The battery life is ≈ 26000 hours.

4.4 Prototype Area

To the right of the RTC there is a small prototype area. Eight test points are provided to connect circuitry from the prototype area to the ATmega328P. With the PICO1TRC rotated 90 degrees clockwise there is a row of six pins at the top and two pins at the bottom. The pinout is shown in Table 3.

Pin Name	**Arduino Number**	**Notes**
GND		left top
SDA (PC4)	A4	
SCL (PC5)	A5	
PB1	9	
PB2	10	
VCC		right top
GND		left bottom
VCC		right bottom

Table 3: Prototype Area Pins

4.5 Debug LED

The debug LED, `D2`, can be connected to `U1` pin 13 (PD7) of the ATmega328P or left disconnected. `U1` pin 13 corresponds to Arduino pin 7

LED jumper in the disconnected position

LED jumper in the PD7 position

4.6 Pinout

The input and output pins for the PICO1TRC are the socket pins of the microcontroller (U1). The pinout is listed in Table 4.

Pin Number	Pin Name	Arduino Number	Notes
2	RXD	0	
3	TXD	1	
4	PD2	2	
5	PD3	3	
6	PD4	4	
11	PD5	5	
12	PD6	6	
13	PD7	7	Debug LED
14	PB0	8	
15	PB1	9	
16	PB2	10	
17	PB3	11	MOSI
18	PB4	12	MISO
19	PB5	13	SCK
23	PC0	A0	
24	PC1	A1	
25	PC2	A2	
26	PC3	A3	
27	PC4	A4	SDA
28	PC5	A5	SCL
1	Reset		
9	XTAL1		PB6
10	XTAL2		PB7
7	VCC		
20	AVCC		
21	AREF		
8	GND		
22	GND		

Table 4: U1 Pinout

5 Programming the PICO1TRC

The PICO1TRC can be programmed using the Arduino tools (version 0011 or later).

5.1 Selecting the proper board

In order for the Arduino tools to recognize the wiblocks boards additional lines need to be added to the boards.txt file. The additional lines are shown in Listing 1 (with annotations). A file containing these adddions can be downloaded from wiblocks. Once boards.txt is modified select wiblocks 328 at 12MHz from the Tools->Board menu.

5.2 Downloading a program

The PICO1TRC must be rebooted to start the program download. This can be done by pressing the reset button S1 immediately before starting the download. If your USB port is configured to set RTS on close then the reset will occur automatically.

Listing 1: boards.txt Modifications for the PICO1TRC

```
1  wiblocks_328.name=wiblocks 328 at 12MHz
2  wiblocks_328.upload.protocol=stk500
3  wiblocks_328.upload.maximum_size=30720
4  wiblocks_328.upload.speed=19200
5  wiblocks_328.bootloader.low_fuses=0xff
6  wiblocks_328.bootloader.high_fuses=0xdd
7  wiblocks_328.bootloader.extended_fuses=0x00
8  wiblocks_328.bootloader.path=atmega328
9  wiblocks_328.bootloader.file=wiblocks_328.hex
10 wiblocks_328.bootloader.unlock_bits=0x3F
11 wiblocks_328.bootloader.lock_bits=0x0F
12 wiblocks_328.build.mcu=atmega328p
13 wiblocks_328.build.f_cpu=12000000L
14 wiblocks_328.build.core=arduino
```

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Atmel. (2009b). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. 314. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)

Atmel. (2009c). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)

Maxim. (2009a, July). DS1337 I2C Serial Real-Time Clock. 2-3. (Retrieved September 30, 2009, from http://datasheets.maxim-ic.com/en/ds/DS1337-DS1337C.pdf)

Maxim. (2009b, July). DS1337 I2C Serial Real-Time Clock. (Retrieved September 30, 2009, from http://datasheets.maxim-ic.com/en/ds/DS1337-DS1337C.pdf)

6 Assembly Documentation and Schematics

Table 5: Bill of Materials

Kit: PICO1TRC-KIT

Qty	Reference	Part Number	Description
1	B21	CON_BAT__Keystone_500	connector, battery, CR1220
5	C1, C2, C3, C13, C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
2	C5, C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
2	C10, C11	CAPPR__Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
1	D1	DIOA-1N4148	diode, 1N4148
1	D2	LEDR-1T-GRN-2M00	LED, T1, Green
2	D21, D22	DIOA-BAT41	diode, BAT41
1	J3	HDR_BR-3X1-100M	header, 3x1, 100mils
1	J5	HDR_BR-6X1-100M	header, 6x1, 100mils
1	J10	CON__CUI-PJ-202AH	power jack, 2.1mm
1	L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
4	R1, R3, R22, R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
1	R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
1	R10	RES-124R-0W125-1T00	resistor, 124 Ohm, 1/8W, 1%
1	R11	RES-205R-0W125-1T00	resistor, 205 Ohm, 1/8W, 1%
1	S1	SW__Panasonic_EVQ-PAE04M	pushbutton
1	U1	IC__ATMEL_ATmega168-20PU	ATmega168-20PU
1	U10	VREG__On-Semi_MC33269TG	voltage regulator, adj, 800mA, TO-220
1	U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1377+
1	X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
1	X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
1		DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
1		JMP__Adamtech_MSBHG	Shunt with handle
1		DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
1		wiblock_PICO1TRC-PCB	
1		RES-1K00-0W125-1T00	resistor, 1K, 1/8W, 1%

Table 6: Component List

Kit: PICO1TRC-KIT

Reference	Part Number	Description
B21	CON_BAT__Keystone_500	connector, battery, CR1220
C1	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C2	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C3	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C13	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C5	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C10	CAPPR__Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
C11	CAPPR__Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
D1	DIOA-1N4148	diode, 1N4148
D2	LEDR-1T-GRN-2M00	LED, T1, Green
D21	DIOA-BAT41	diode, BAT41
D22	DIOA-BAT41	diode, BAT41
J3	HDR_BR-3X1-100M	header, 3x1, 100mils
J5	HDR_BR-6X1-100M	header, 6x1, 100mils
J10	CON__CUI-PJ-202AH	power jack, 2.1mm
L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
R1	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R3	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R22	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
R10	RES-124R-0W125-1T00	resistor, 124 Ohm, 1/8W, 1%
R11	RES-205R-0W125-1T00	resistor, 205 Ohm, 1/8W, 1%
S1	SW__Panasonic_EVQ-PAE04M	pushbutton
U1	IC__ATMEL_ATmega168-20PU	ATmega168-20PU
U10	VREG__On-Semi_MC33269TG	voltage regulator, adj, 800mA, TO-220
U23	IC_RTC__Maxim_DS1337+	IC, RTC, DS1377+
X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
	DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
	JMP__Adamtech_MSBHG	Shunt with handle
	DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
	wiblock_PICO1TRC-PCB	
	RES-1K00-0W125-1T00	resistor, 1K, 1/8W, 1%

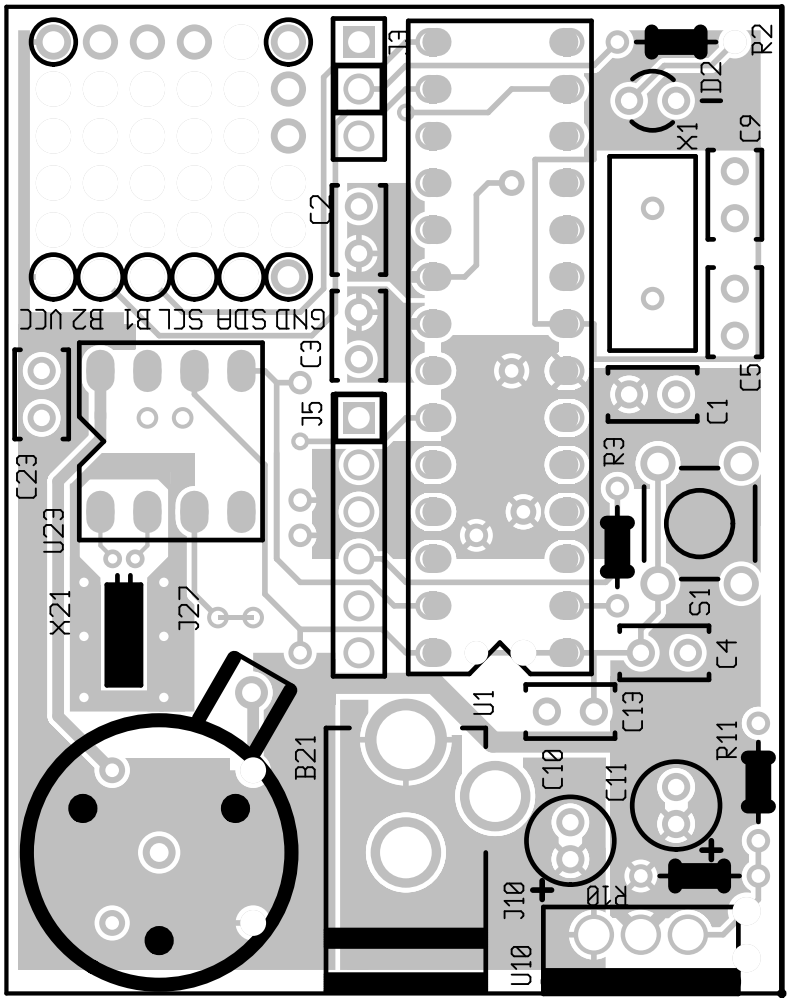


Figure 1: PICO1TRC Top Side Assembly Drawing (Rev 0)

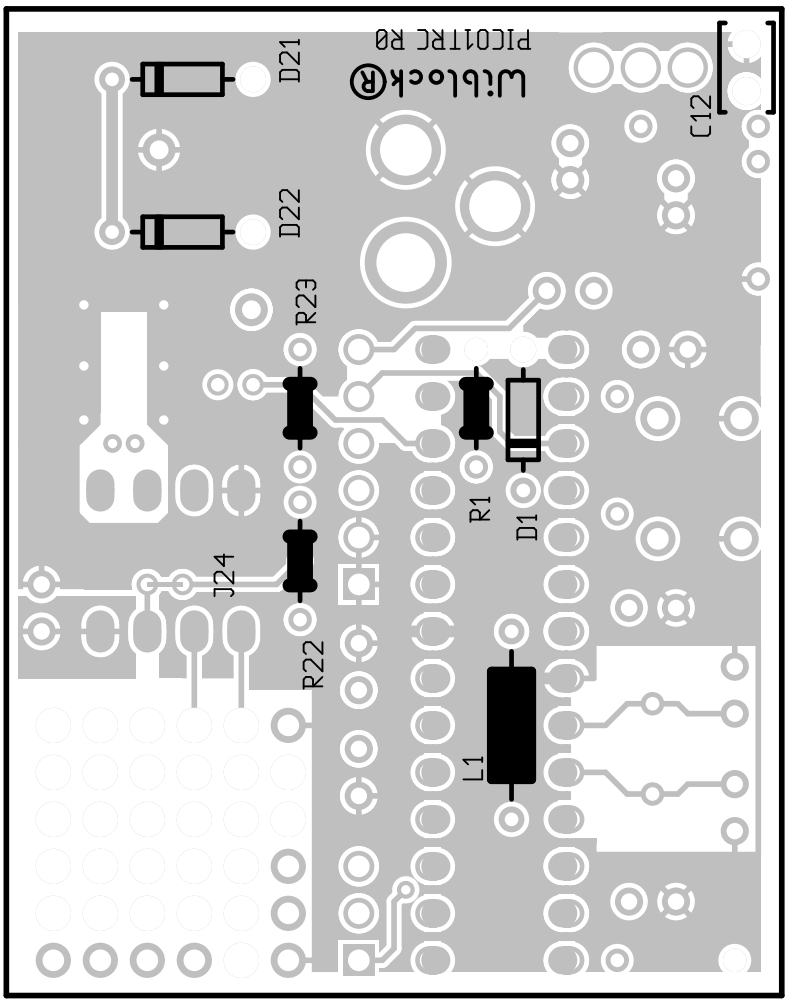


Figure 2: PICO1TRC Bottom Side Assembly Drawing (Rev 0)

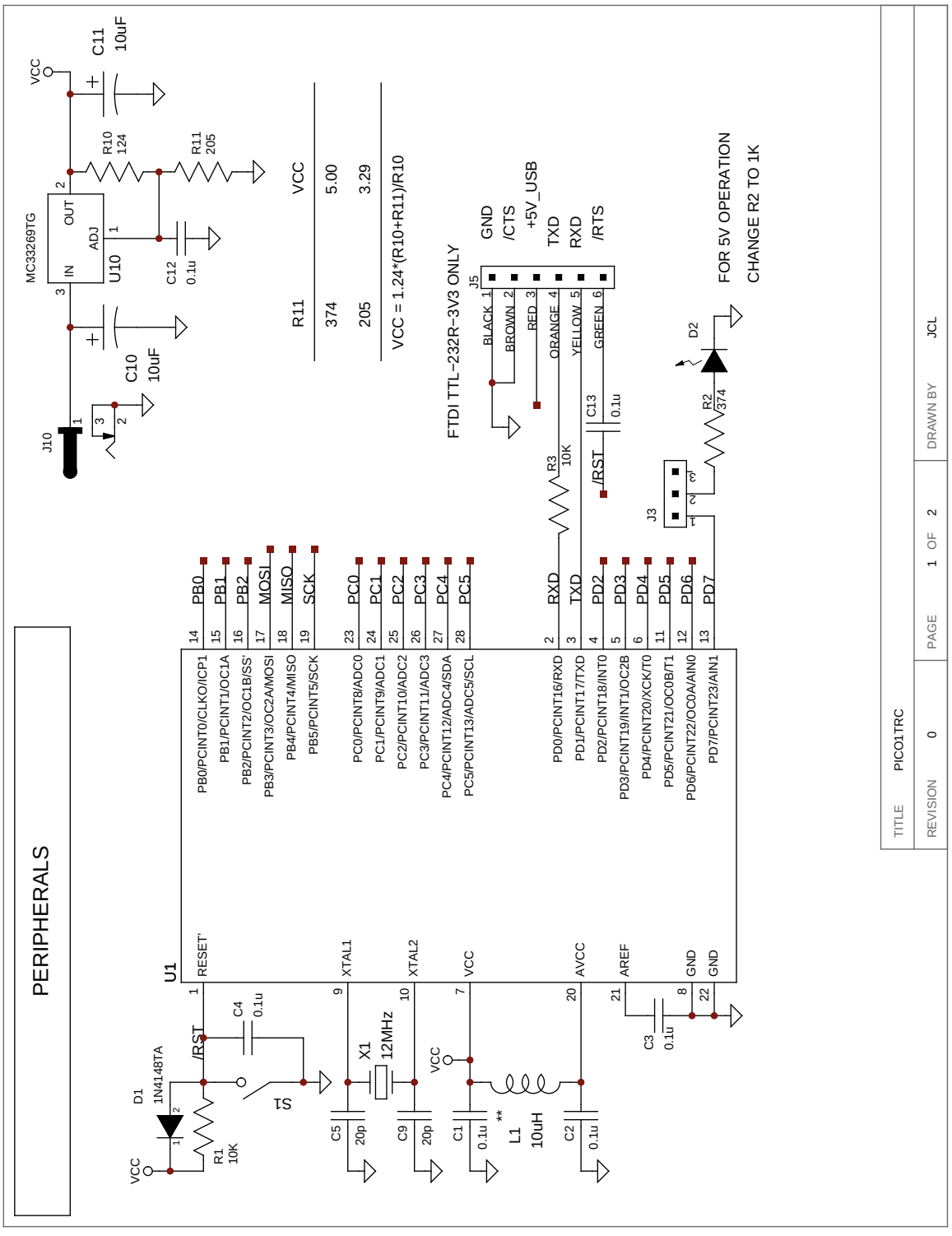


Figure 3: PICO1TRC (Rev 0)

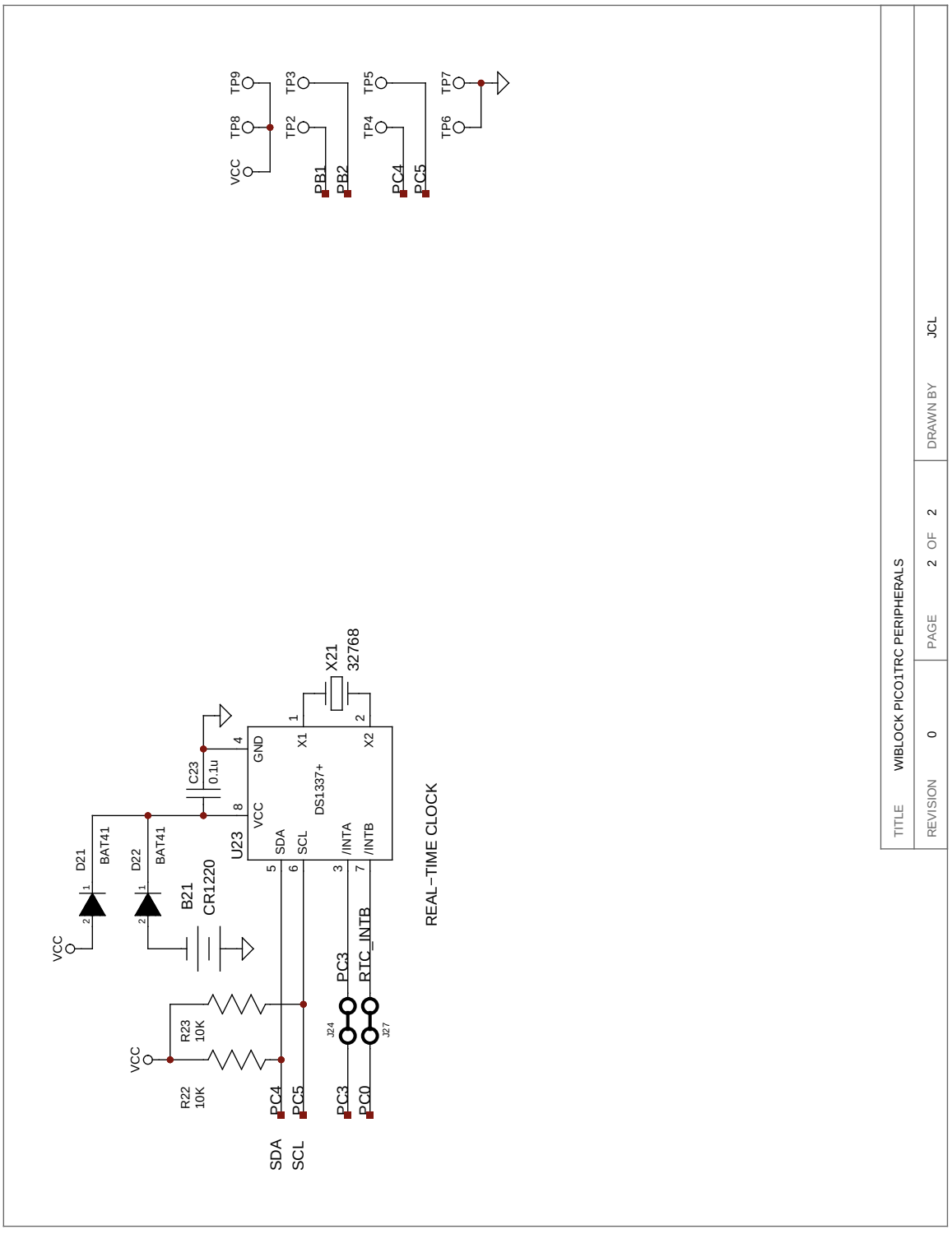


Figure 4: PICO1TRC (Rev 0)

19-4652; 7/09

DS1337
I²C Serial Real-Time Clock

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I^2C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The device is fully accessible through the serial interface while V_{CC} is between 1.8V and 5.5V. I^2C operation is not guaranteed below 1.8V. Timekeeping operation is maintained with V_{CC} as low as 1.3V.

APPLICATIONS

Handhelds (GPS, POS Terminal, MP3 Player)

Consumer Electronics (Set-Top Box, VCR/Digital Recording)

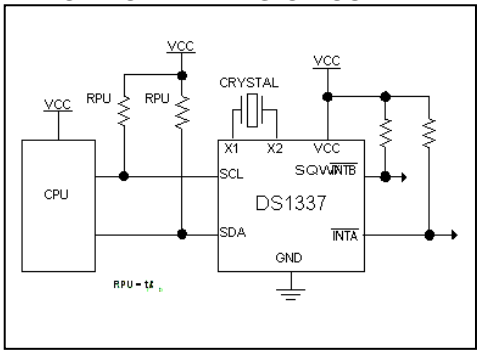
Office Equipment (Fax/Printer, Copier)

Medical (Glucometer, Medicine Dispenser)

Telecommunications (Router, Switch, Server)

Other (Utility Meter, Vending Machine, Thermostat, Modem)

TYPICAL OPERATING CIRCUIT



FEATURES

- **Real-Time Clock (RTC) Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Valid Up to 2100**
- **Available in a Surface-Mount Package with an Integrated Crystal (DS1337C)**
- **I^2C Serial Interface**
- **Two Time-of-Day Alarms**
- **Oscillator Stop Flag**
- **Programmable Square-Wave Output Defaults to 32kHz on Power-Up**
- **Available in 8-Pin DIP, SO, or µSOP**
- **-40°C to +85°C Operating Temperature Range**

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1337+	-40°C to +85°C	8 DIP (300 mils)	DS1337
DS1337S+	-40°C to +85°C	8 SO (150 mils)	DS1337
DS1337U+	-40°C to +85°C	8 µSOP	1337
DS1337C#	-40°C to +85°C	16 SO (300 mils)	DS1337C

+ Denotes a lead(Pb)-free/RoHS-compliant device.
 # Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes.
† A "+" anywhere on the top mark denotes a lead-free device. A "#" denotes a RoHS-compliant device.

Pin Configurations appear at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..….-0.3V to +6.0V
Operating Temperature Range (Noncondensing)……..…….-40°C to +85°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	Full operation	1.8	3.3	5.5	V
	V_{CCT}	Timekeeping (Note 5)	1.3		1.8	V
Logic 1	V_{IH}	SCL, SDA	0.7 x V_{CC}		V_{CC} + 0.3	V
		$\overline{INTA}$, SQW/$\overline{INTB}$			5.5	
Logic 0	V_{IL}		-0.3		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS—Full Operation

(**V_{CC} = 1.8V to 5.5V**, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}	(Note 2)	-1		+1	µA
I/O Leakage	I_{LO}	(Note 3)	-1		+1	µA
Logic 0 Output (V_{OL} = 0.4V)	I_{OL}	(Note 3)			3	mA
Active Supply Current	I_{CCA}	(Note 4)			150	µA
Standby Current	I_{CCS}	(Notes 5, 6)			1.5	µA

DC ELECTRICAL CHARACTERISTICS--Timekeeping

(**V_{CC} = 1.3V to 1.8V,** T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timekeeping Current (Oscillator Enabled)	I_{CCTOSC}	(Notes 5, 7, 8, 9)		425	600	nA
Data-Retention Current (Oscillator Disabled)	I_{CCTDDR}	(Notes 5, 9)			100	nA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.8V to 5.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 10)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time (Notes 11, 12)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 13)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 14)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 14)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 14)			400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 15)			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}			100		ms

Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: SCL only.

Note 3: SDA, $\overline{INTA}$, and SQW/$\overline{INTB}$.

Note 4: I_{CCA}—SCL clocking at max frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 5: Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 6: SQW enabled.

Note 7: Specified with the SQW function disabled by setting INTCN = 1.

Note 8: Using recommended crystal on X1 and X2.

Note 9: The device is fully accessible when $1.8 \le V_{CC} \le 5.5V$. Time and date are maintained when $1.3V \le V_{CC} \le 1.8V$.

Note 10: After this period, the first clock pulse is generated

Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 12: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 13: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \ge$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,max} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

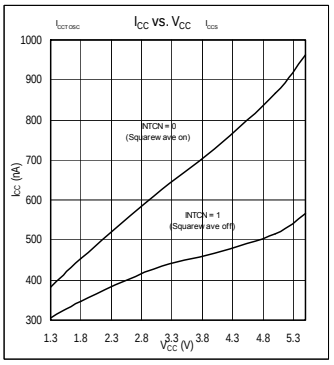
Note 14: C_B—total capacitance of one bus line in pF.

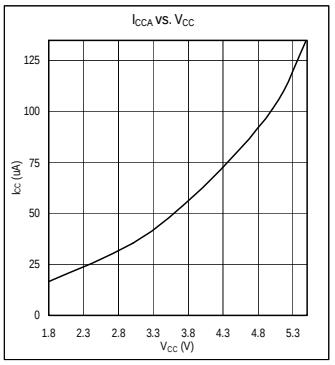
Note 15: Guaranteed by design. Not production tested.

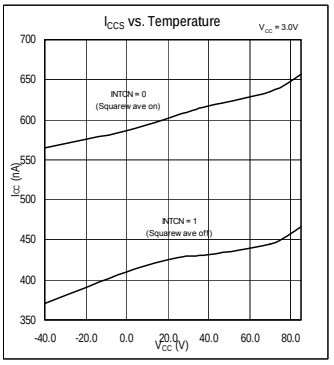
Note 16: The parameter t_{OSF} is the period of time that the oscillator must be stopped for the OSF bit to be set over the voltage range of $V_{CC(MIN)} \le V_{CC} \le V_{CC(MAX)}$.

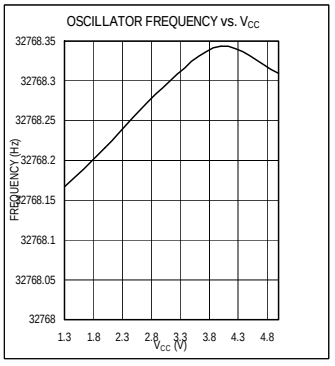
TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)





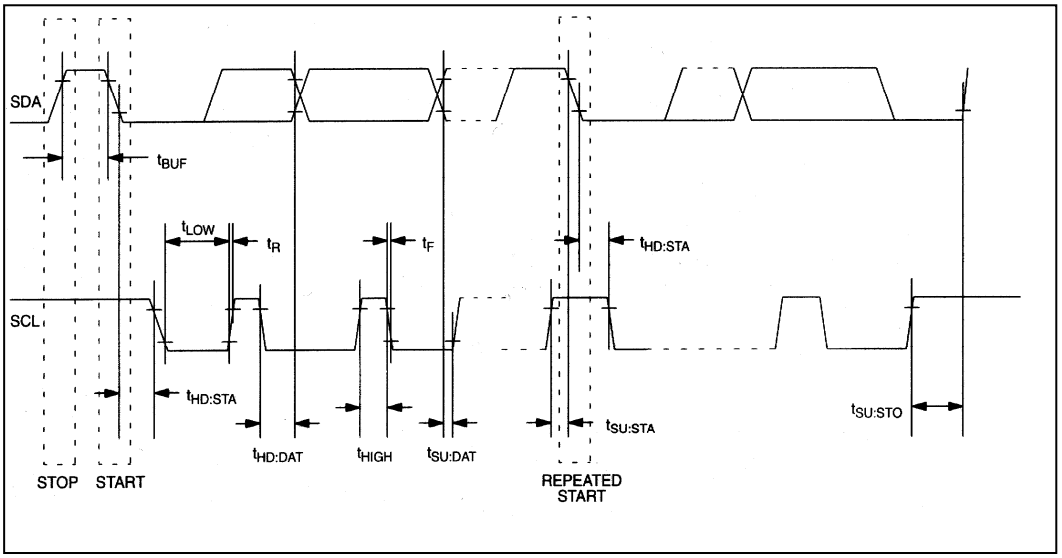




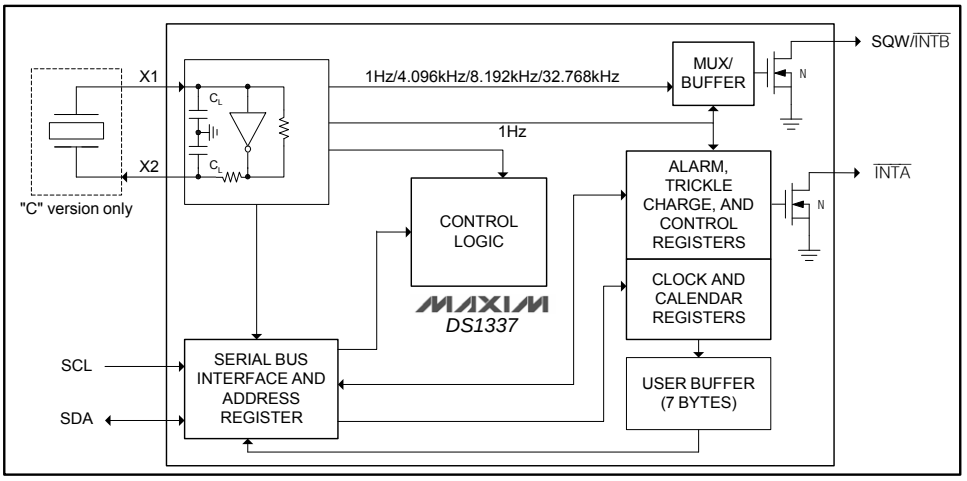
PIN DESCRIPTION

PIN		NAME	FUNCTION
8	16		
1	—	X1	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*. An external 32.768kHz oscillator can also drive the DS1337. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
2	—	X2	
3	14	$\overline{INTA}$	Interrupt Output. When enabled, $\overline{INTA}$ is asserted low when the time/day/date matches the values set in the alarm registers. This pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
4	15	GND	Ground. DC power is provided to the device on this pin.
5	16	SDA	Serial Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is open-drain output and requires an external pullup resistor.
6	1	SCL	Serial Clock Input. SCL is used to synchronize data movement on the serial interface.
7	2	SQW/$\overline{INTB}$	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left floating.
8	3	V_{CC}	DC Power. DC power is provided to the device on this pin.
—	4–13	N.C.	No Connect. These pins are not connected internally, but must be grounded for proper operation.

TIMING DIAGRAM



BLOCK DIAGRAM



DETAILED DESCRIPTION

The *Block Diagram* shows the main elements of the DS1337. As shown, communications to and from the DS1337 occur serially over an I²C bus. The DS1337 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible through the I²C interface whenever V_{CC} is between 5.5V and 1.8V. I²C operation is not guaranteed when V_{CC} is below 1.8V. The DS1337 maintains the time and date when V_{CC} is as low as 1.3V.

OSCILLATOR CIRCUIT

The DS1337 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 1. Crystal Specifications*

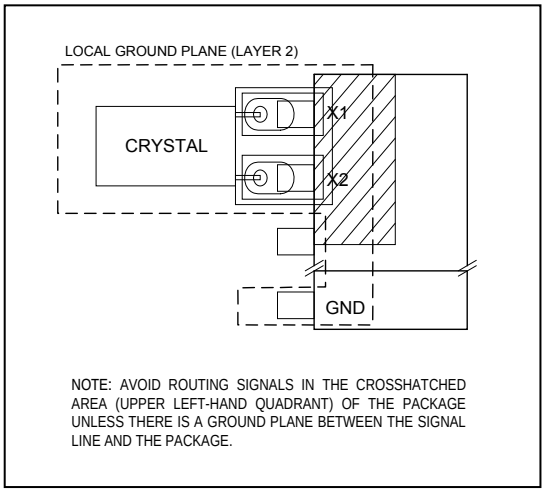
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 1 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Figure 1. Typical PC Board Layout for Crystal



DS1337C ONLY

The DS1337C integrates a standard 32,768Hz crystal in the package. Typical accuracy at nominal V_{CC} and +25°C is approximately +10ppm. Refer to *Application Note 58* for information about crystal accuracy vs. temperature.

OPERATING MODES

The amount of current consumed by the DS1337 is determined, in part, by the I²C interface and oscillator operation. The following table shows the relationship between the operating mode and the corresponding I_{CC} parameter.

Operating Mode	V_{CC}	Power
I²C Interface Active	$1.8V \le V_{CC} \le 5.5V$	I_{CC} Active (I_{CCA})
I²C Interface Inactive	$1.8V \le V_{CC} \le 5.5V$	I_{CC} Standby (I_{CCS})
I²C Interface Inactive	$1.3V \le V_{CC} \le 1.8V$	Timekeeping (I_{CCTOSC})
I²C Interface Inactive Oscillator Disabled	$1.3V \le V_{CC} \le 1.8V$	Data Retention (I_{CCTDDR})

ADDRESS MAP

Table 2 shows the address map for the DS1337 registers. During a multibyte access, when the address pointer reaches the end of the register space (0Fh) it wraps around to location 00h. On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 2. Timekeeper Registers

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Minutes			Minutes				Minutes	00–59
02H	0	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hour				Hours	1–12 +AM/PM 00–23
			10 Hour							
03H	0	0	0	0	0	Day			Day	1–7
04H	0	0	10 Date		Date				Date	01–31
05H	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06H	10 Year				Year				Year	00–99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09H	A1M3	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
			10 Hour							
0AH	A1M4	DY/$\overline{DT}$	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	01–31
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0CH	A2M3	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/PM 00–23
			10 Hour							
0DH	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	01–31
0EH	$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	—

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied or V_{CC} falls below the V_{OSC}.*

I²C INTERFACE

The I²C interface is accessible whenever V_{CC} is at a valid level. If a microcontroller connected to the DS1337 resets while reading from the DS1337 during an I²C read, the two could become unsynchronized. The microcontroller must terminate the last byte read with a Not-Acknowledge (NACK) to properly terminate the read. When the microcontroller resets, the DS1337 I²C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Table 2. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enable, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The DS1337 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). All hours values, including the alarms, must be reinitialized whenever the 12/$\overline{24}$-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99–00.

ALARMS

The DS1337 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h–0Ah. Alarm 2 can be set by writing to registers 0Bh–0Dh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes—each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 3 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. The bit(s) will remain at a logic 1 until written to a logic 0 by the user. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{INTA}$ or SQW/$\overline{INTB}$) signals. The match is tested on the once-per-second update of the time and date registers.

Table 3. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL-PURPOSE REGISTERS

The DS1337 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator ($\overline{EOSC}$). This active-low bit when set to logic 0 starts the oscillator. When this bit is set to logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

SQW/$\overline{INTB}$ Output

INTCN	RS2	RS1	SQW/$\overline{INTB}$ OUTPUT	A2IE
0	0	0	1Hz	X
0	0	1	4.096kHz	X
0	1	0	8.192kHz	X
0	1	1	32.768kHz	X
1	X	X	$\overline{A2F}$	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers l activates the $\overline{INTA}$ pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/$\overline{INTB}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{INTB}$ pin. This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INTA}$ (when INTCN = 0) or to assert SQW/$\overline{INTB}$ (when INTCN = 1). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INTA}$. When the A1IE bit is set to logic 0, the A1F bit does not initiate the $\overline{INTA}$ signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on V_{CC} is insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on either $\overline{INTA}$ or SQW/$\overline{INTB}$ depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the $\overline{INTA}$ pin goes low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the SQW/$\overline{INTB}$ pin goes low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{INTA}$ pin goes low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

I²C SERIAL DATA BUS

The DS1337 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1337 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS1337 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

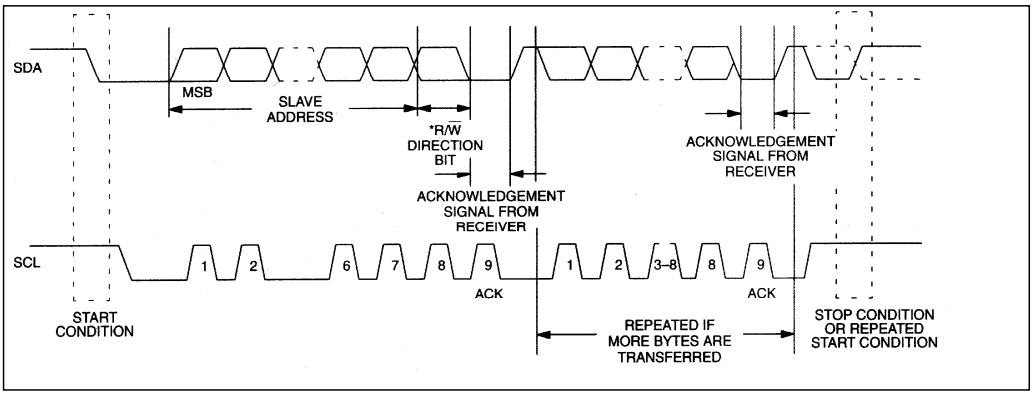
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2. Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1337 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 3). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the DS1337 acknowledges the slave address + write bit, the master transmits a register address to the DS1337. This sets the register pointer on the DS1337. The master may then transmit zero or more bytes of data, with the DS1337 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1337 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 4 and Figure 5). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The DS1337 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1337 must receive a “not acknowledge” to end a read.

Figure 3. Data Write—Slave Receiver Mode

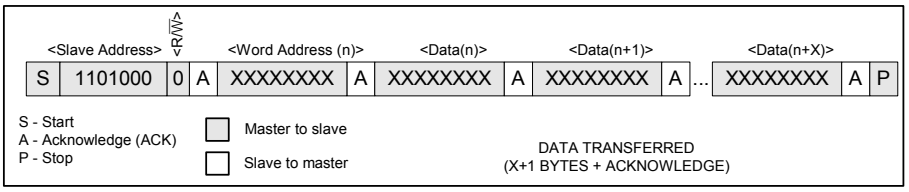


Figure 4. Data Read (from Current Pointer Location)—Slave Transmitter Mode

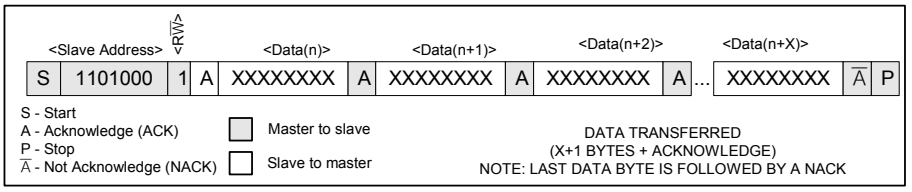
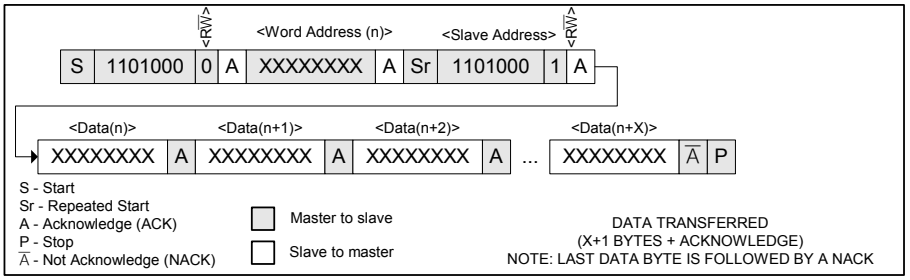


Figure 5. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



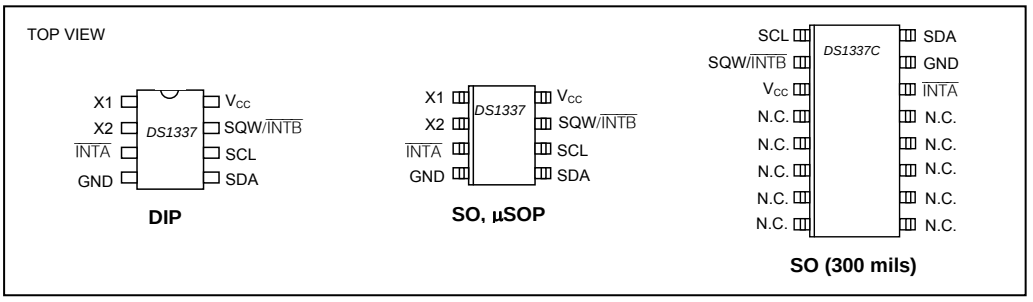
HANDLING, PC BOARD LAYOUT, AND ASSEMBLY

The DS1337C package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

PIN CONFIGURATIONS



CHIP INFORMATION

TRANSISTOR COUNT: 10,950
PROCESS: CMOS

THERMAL INFORMATION

PACKAGE	THETA-J_A (°C/W)	THETA-J_C (°C/W)
8 DIP	110	40
8 SO	170	40
8 µSOP	229	39
16 SO	73	23

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 PDIP	P8+8	**21-0043**
8 SO	S8+2	**21-0041**
8 µMAX	U8+1	**21-0036**
16 SO	W16-H2	**21-0042**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
080508	Added device access details to *General Description* section.	1
	Removed leaded ordering numbers from the *Ordering Information* table.	1
	Added Note 5 to Timekeeping V_{CC} EC table range.	2
	Added “Full Operation” and “Timekeeping” to headers to clarify table usage.	2
	Added OSF parameter to EC table.	3
	Updated *Pin Description* to indicate max input voltage and that unused outputs may be left open.	5
	Added oscillator circuit and show open-drain transistors on *Block Diagram*.	6
	Added *Operating Mode* section with details on operating mode and corresponding Icc parameter.	7
	Added *I²C Interface* section explaining how to synchronize a microcontroller and the RTC.	8
	Corrected legend in figure 5 for not-acknowledge (add overbar to symbol).	14
071609	Removed conflicting SDA/SCL input bias statement in *Pin Description*.	5

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

MC33269, NCV33269

800 mA, Adjustable Output, Low Dropout Voltage Regulator

The MC33269/NCV33269 series are low dropout, medium current, fixed and adjustable, positive voltage regulators specifically designed for use in low input voltage applications. These devices offer the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum.

The regulator consists of a 1.0 V dropout composite PNP−NPN pass transistor, current limiting, and thermal shutdown.

Features

- 3.3 V, 5.0 V, 12 V and Adjustable Versions
  2.85 V version available as MC34268
- Space Saving DPAK, SO−8 and SOT−223 Power Packages
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.0% Tolerance
- Pb−Free Packages are Available
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC33269D	Adj	MC33269D−5.0	5.0 V
MC33269DT	Adj	MC33269DT−5.0	5.0 V
NCV33269DTRK*	Adj	MC33269T−5.0	5.0 V
MC33269T	Adj		
MC33269D−3.3	3.3 V	MC33269D−012	12 V
MC33269DT−3.3	3.3 V	MC33269DT−012	12 V
NCV33269DTRK−3.3*	3.3 V	NCV33269DTRK−012*	12 V
MC33269T−3.3	3.3 V	MC33269T−012	12 V
MC33269ST−3.3	3.3 V		

*NCV prefix is for automotive and other applications requiring site and change control.

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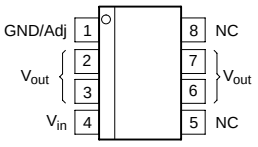
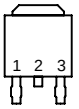
SO−8
D SUFFIX
CASE 751



(Top View)

DPAK
DT SUFFIX
CASE 369C



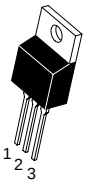
(Top View)

1. GND/Adj
2. V_{out}
3. V_{in}

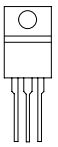
SOT−223
ST SUFFIX
CASE 318E

(Top View)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.



TO−220AB
T SUFFIX
CASE 221AB



(Top View)

1. GND/Adj
2. V_{out}
3. V_{in}

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

MAXIMUM RATINGS

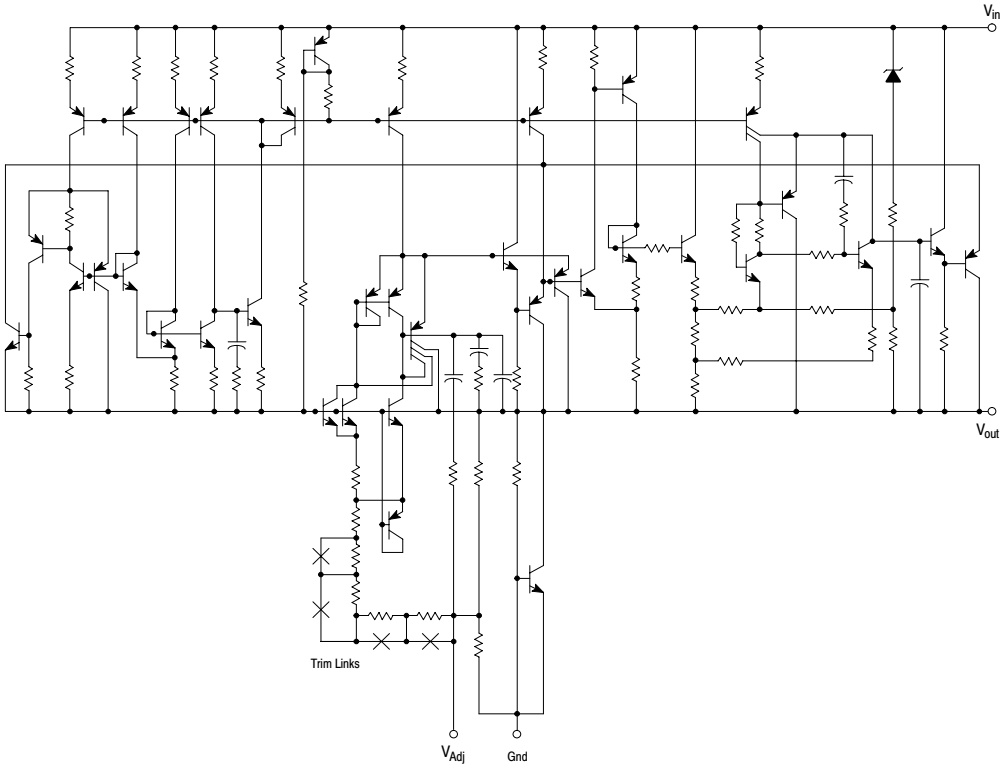
Rating		Symbol	Value	Unit
Power Supply Input Voltage		V_{in}	20	V
Power Dissipation				
Case 369C (DPAK)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	92	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	6.0	°C/W
Case 751 (SO−8)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	160	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	25	°C/W
Case 221A (TO−220)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	65	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	5.0	°C/W
Case 318E (SOT−223)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	156	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	15	°C/W
Operating Die Junction Temperature Range		T_J	−40 to +150	°C
Operating Ambient Temperature Range	MC33269	T_A	−40 to +125	°C
	NCV33269		−40 to +125	
Storage Temperature		T_{stg}	−55 to +150	°C
Electrostatic Discharge Sensitivity (ESD)	Human Body Model (HBM)	ESD	4000	V
	Machine Model (MM)		400	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (C_O = 10 μF, T_A = 25°C, for min/max values T_A = −40°C to +125°C, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage (I_{out} = 10 mA, T_A = 25°C)		V_O				V
	3.3 Suffix (V_{CC} = 5.3 V)		3.27	3.3	3.33	
	5.0 Suffix (V_{CC} = 7.0 V)		4.95	5.0	5.05	
	12 Suffix (V_{CC} = 14 V)		11.88	12	12.12	
Output Voltage (Line, Load and Temperature) (Note 1) (1.25 V ≤ V_{in} − V_{out} ≤ 15 V, I_{out} = 500 mA) (1.35 V ≤ V_{in} − V_{out} ≤ 10 V, I_{out} = 800 mA)		V_O				V
	3.3 Suffix		3.23	3.3	3.37	
	5.0 Suffix		4.9	5.0	5.1	
	12 Suffix		11.76	12	12.24	
Reference Voltage for Adjustable Voltage (I_{out} = 10 mA, V_{in} − V_{out} = 2.0 V, T_A = 25°C)		V_{ref}	1.235	1.25	1.265	V
Reference Voltage (Line, Load and Temperature) (Note 1) for Adjustable Voltage (1.25 V ≤ V_{in} − V_{out} ≤ 15 V, I_{out} = 500 mA) (1.35 V ≤ V_{in} − V_{out} ≤ 10 V, I_{out} = 800 mA)		V_{ref}	1.225	1.25	1.275	V
Line Regulation	(I_{out} = 10 mA, V_{in} = [V_{out} + 1.5 V] to V_{in} = 20 V, T_A = 25°C)	Reg_{line}	−	−	0.3	%
Load Regulation	(V_{in} = V_{out} + 3.0 V, I_{out} = 10 mA to 800 mA, T_A = 25°C)	Reg_{load}	−	−	0.5	%
Dropout Voltage	(I_{out} = 500 mA)	V_{in} − V_{out}	−	1.0	1.25	V
	(I_{out} = 800 mA)		−	1.1	1.35	
Ripple Rejection	(10 V_{pp}, 120 Hz Sinewave; I_{out} = 500 mA)	RR	55	−	−	dB
Current Limit	(V_{in} − V_{out} = 10 V)	I_{Limit}	800	−	−	mA
Quiescent Current (Fixed Output)	(1.5 V ≤ V_{out} ≤ 3.3 V)	I_Q	−	5.5	8.0	mA
	(5 V ≤ V_{out} ≤ 12 V)		−	−	20	
Minimum Required Load Current	Fixed Output Voltage	I_{Load}	−	−	0	mA
	Adjustable Voltage		8.0	−	−	
Adjustment Pin Current		I_{Adj}	−	−	120	μA

1. The MC33269−12, V_{in} − V_{out} is limited to 8.0 V maximum, because of the 20 V maximum rating applied to V_{in}.



This device contains 38 active transistors.

Figure 1. Internal Schematic

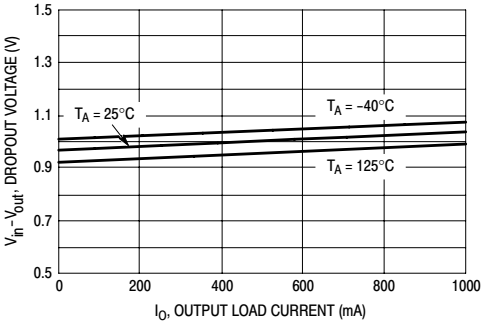


Figure 2. Dropout Voltage versus Output Load Current

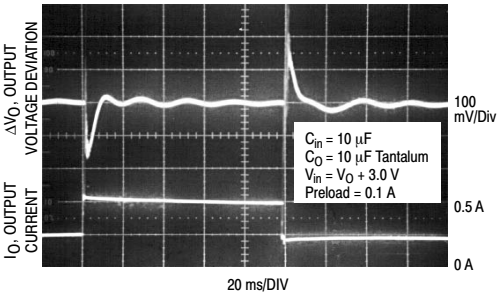


Figure 3. Transient Load Regulation

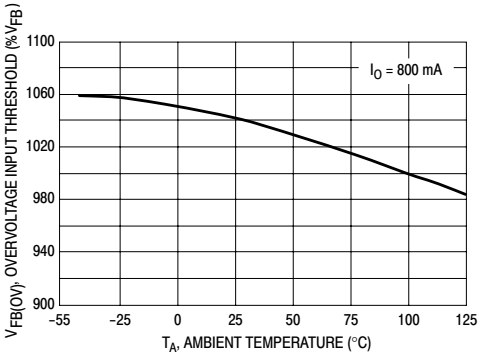


Figure 4. Dropout Voltage versus Temperature

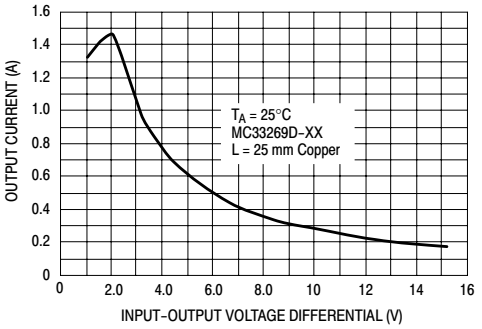


Figure 5. MC33269−XX Output DC Current versus Input−Output Differential Voltage

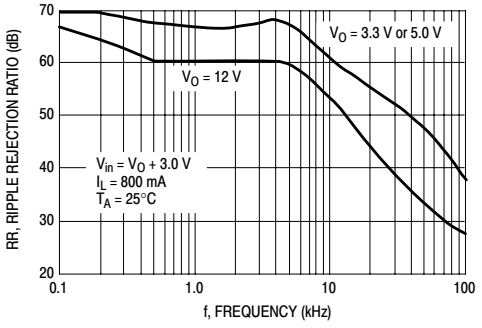


Figure 6. MC33269 Ripple Rejection versus Frequency

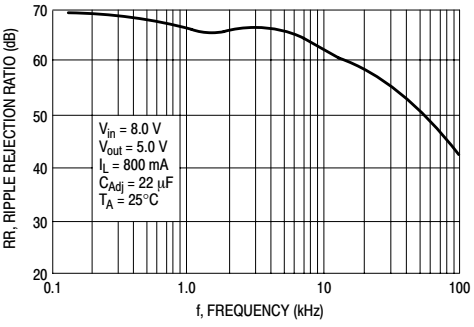


Figure 7. MC33269−ADJ Ripple Rejection versus Frequency

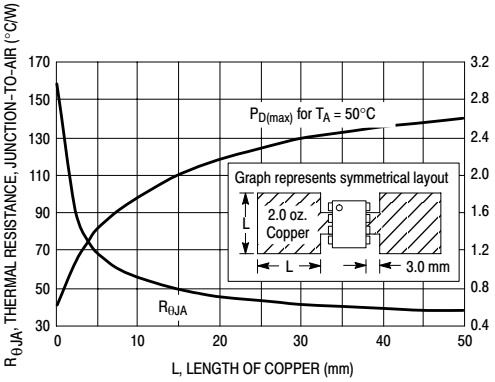


Figure 8. SOP−8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

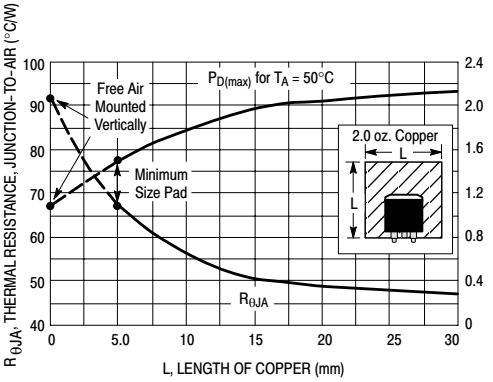


Figure 9. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

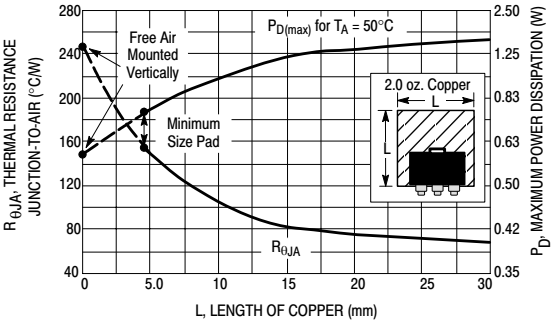


Figure 10. SOT−223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

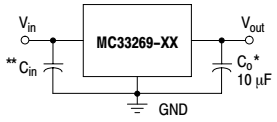
APPLICATIONS INFORMATION

Figures 11 through 15 are typical application circuits. The output current capability of the regulator is in excess of 800 mA, with a typical dropout voltage of less than 1.0 V. Internal protective features include current and thermal limiting.

* The MC33269 requires an external output capacitor for stability. The capacitor should be at least 10 μF with an equivalent series resistance (ESR) of less than 10 Ω but greater than 0.2 Ω over the anticipated operating temperature range. With economical electrolytic capacitors, cold temperature operation can pose a problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Also capacitance and ESR of a solid tantalum capacitor is more stable over temperature. The use of a low ESR ceramic capacitor placed within close proximity to the output of the device could cause instability.

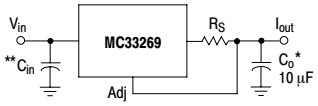
** An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths. This will reduce the circuit's sensitivity to the input line impedance at high frequencies. A 0.33 μF or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. **Applications should be tested over all operating conditions to insure stability.**

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heat−sinking.**



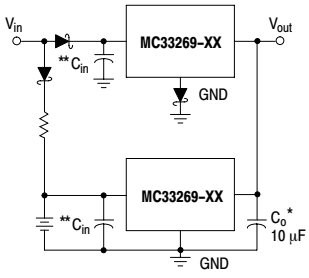
An input capacitor is not necessary for stability, however it will improve the overall performance.

Figure 11. Typical Fixed Output Application



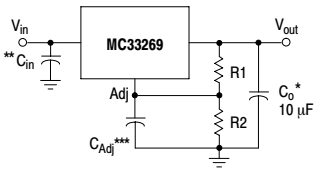
$$I_{out} = \frac{1.25}{R_S}$$

Figure 13. Current Regulator



The Schottky diode in series with the ground leg of the upper regulator shifts its output voltage higher by the forward voltage drop of the diode. This will cause the lower device to remain off until the input voltage is removed.

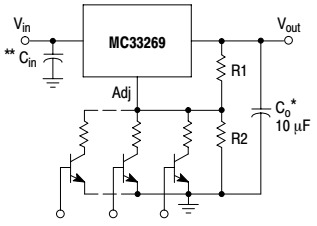
Figure 14. Battery Backed−Up Power Supply



$$V_{out} = 1.25 \left(1 + \frac{R2}{R1}\right) + I_{Adj} R2$$

***C_{Adj} is optional, however it will improve the ripple rejection. The MC34269 develops a 1.25 V reference voltage between the output and the adjust terminal. Resistor R1, operates with constant current to flow through it and resistor R2. This current should be set such that the Adjust Pin current causes negligible drop across resistor R2. The total current with minimum load should be greater than 8.0 mA.

Figure 12. Typical Adjustable Output Application



R_2 sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

Figure 15. Digitally Controlled Voltage Regulator

ORDERING INFORMATION

Device	Package	Shipping Information†
MC33269D	SO−8	98 Units / Rail
MC33269DG	SO−8 (Pb−Free)	
MC33269DR2	SO−8	2500 Units / Tape & Reel
MC33269DR2G	SO−8 (Pb−Free)	
MC33269DT	DPAK	75 Units / Rail
MC33269DTG	DPAK (Pb−Free)	
MC33269DTRK	DPAK	2500 Units / Tape & Reel
MC33269DTRKG	DPAK (Pb−Free)	
MC33269T	TO−220	50 Units / Rail
MC33269TG	TO−220 (Pb−Free)	
MC33269D−3.3	SO−8	98 Units / Rail
MC33269D−3.3G	SO−8 (Pb−Free)	
MC33269DR2−3.3	SO−8	2500 Units / Tape & Reel
MC33269DR2−3.3G	SO−8 (Pb−Free)	
MC33269DT−3.3	DPAK	75 Units / Rail
MC33269DT−3.3G	DPAK (Pb−Free)	
MC33269DTRK−3.3	DPAK	2500 Units / Tape & Reel
MC33269DTRK−3.3G	DPAK (Pb−Free)	
MC33269ST−3.3T3	SOT−223	4000 Units / Tape & Reel
MC33269ST−3.3T3G	SOT−223 (Pb−Free)	
MC33269T−3.3	TO−220	50 Units / Rail
MC33269T−3.3G	TO−220 (Pb−Free)	
MC33269D−5.0	SO−8	98 Units / Rail
MC33269D−5.0G	SO−8 (Pb−Free)	
MC33269DR2−5.0	SO−8	2500 Units / Tape & Reel
MC33269DR2−5.0G	SO−8 (Pb−Free)	
MC33269DT−5.0	DPAK	75 Units / Rail
MC33269DT−5.0G	DPAK (Pb−Free)	
MC33269DTRK−5.0	DPAK	2500 Units / Tape & Reel
MC33269DTRK−5.0G	DPAK (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV prefix is for automotive and other applications requiring site and control changes.

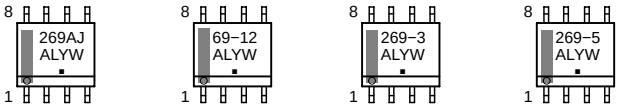
ORDERING INFORMATION (continued)

Device	Package	Shipping Information†
MC33269T−5.0	TO−220	50 Units / Rail
MC33269T−5.0G	TO−220 (Pb−Free)	
MC33269D−012	SO−8	98 Units / Rail
MC33269D−012G	SO−8 (Pb−Free)	
MC33269DR2−012	SO−8	2500 Units / Tape & Reel
MC33269DR2−012G	SO−8 (Pb−Free)	
MC33269DT−012	DPAK	75 Units / Rail
MC33269DT−012G	DPAK (Pb−Free)	
MC33269DTRK−012	DPAK	2500 Units / Tape & Reel
MC33269DTRK−012G	DPAK (Pb−Free)	
MC33269T−012	TO−220	50 Units / Rail
MC33269T−012G	TO−220 (Pb−Free)	
NCV33269DTRK*	DPAK	2500 Units / Tape & Reel
NCV33269DTRKG*	DPAK (Pb−Free)	
NCV33269DTRK−3.3*	DPAK	
NCV33269DTRK−3.3G*	DPAK (Pb−Free)	
NCV33269DTRK−012*	DPAK	
NCV33269DTRK−012G*	DPAK (Pb−Free)	

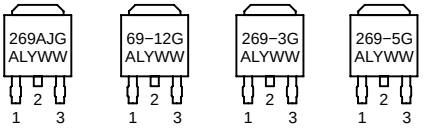
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV prefix is for automotive and other applications requiring site and control changes.

MARKING DIAGRAMS

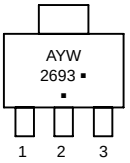
SO−8
D SUFFIX
CASE 751



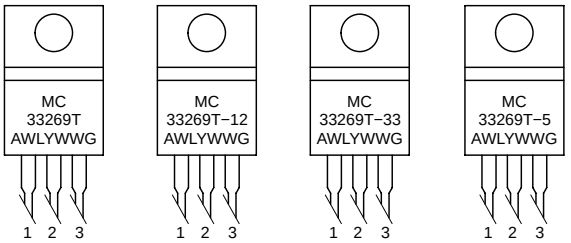
DPAK
DT SUFFIX
CASE 369C



SOT−223
ST SUFFIX
CASE 318E



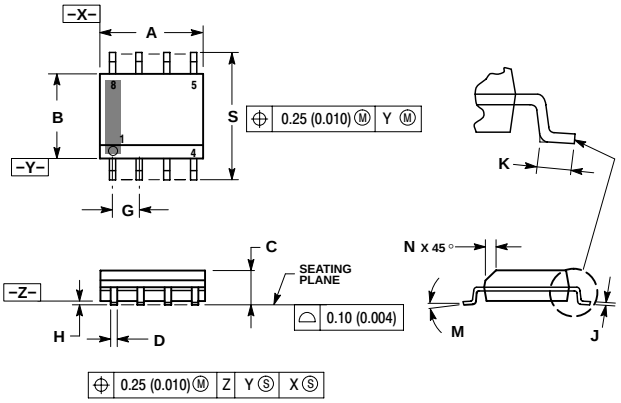
TO−220AB
T SUFFIX
CASE 221A



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G = Pb−Free Package
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PACKAGE DIMENSIONS

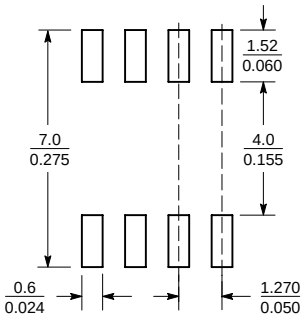
SO−8
D SUFFIX
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

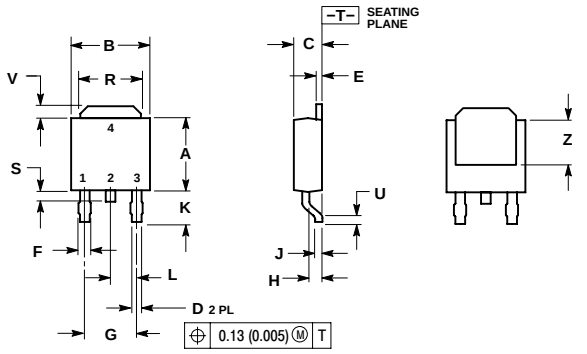


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

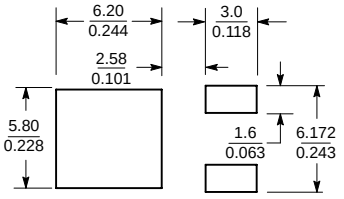
DPAK
DT SUFFIX
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

SOLDERING FOOTPRINT*

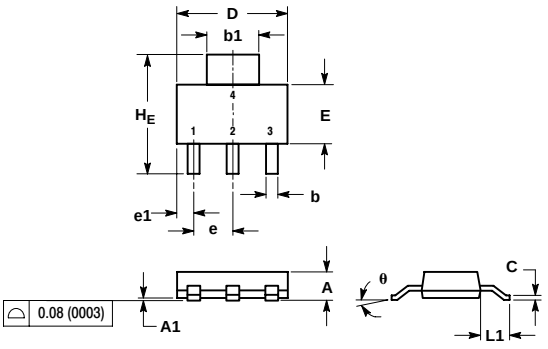


SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

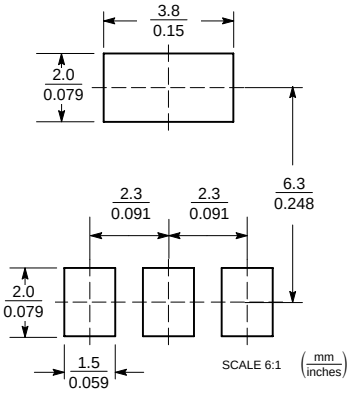
SOT−223
ST SUFFIX
CASE 318E−04
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

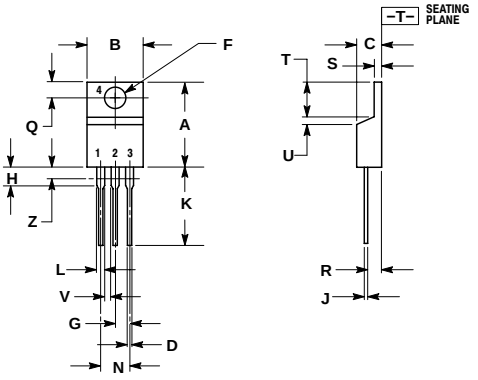
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TO−220AB, SINGLE GAUGE
T SUFFIX
CASE 221AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.055	0.508	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

PUBLICATION ORDERING INFORMATION

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