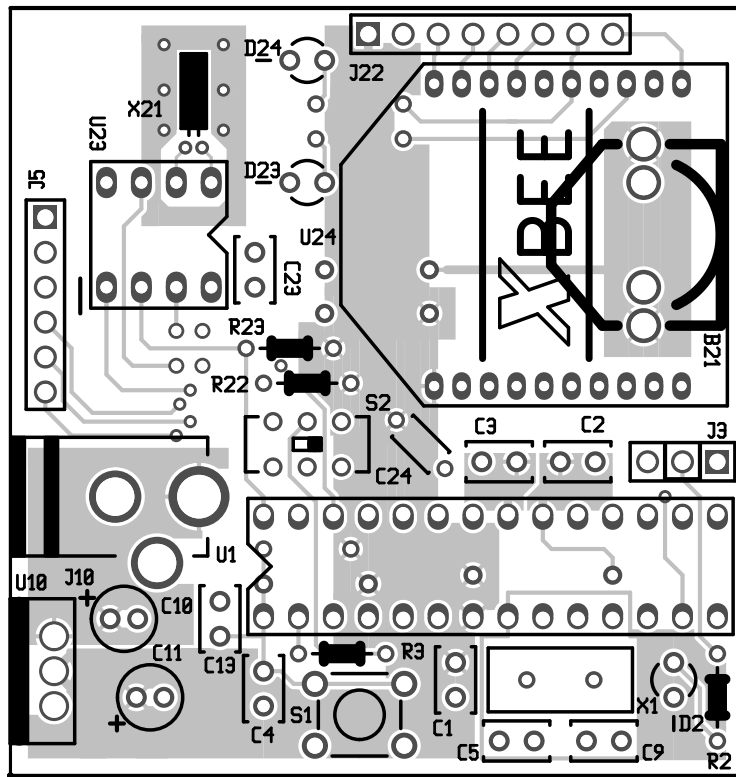


PRELIMINARY



PICOBEE Description

The PICOBEE is a low-cost microcontroller development board that is compatible with the Arduino development tools. The board includes an XBee interface and a real-time clock with battery backup. The board is 2.1" x 2.2" and contains pins for all the ATmega328 and XBee I/O pins.

Features

- 2.1" x 2.2"
- XBee interface
- Real-time Clock with two alarms and battery backup
- Replaceable and upgradeable CPU
- Compatible with the Arduino development tools.
- ATmega328P running at 12MHz
- Two rows of 14 pins (300mil spacing) with all ATmega328 I/O functions.
- Six pin header for FTDI TTL-232R-3V3 cable.
- Debug LED that can be jumpered to Pin 7 or disconnected.
- A/D reference supply filtered per Atmel specification.
- Reset circuit per Atmel specification.

PRELIMINARY

1 Assembling the PICOBEE

⚠ Semiconductors are electrostatic-sensitive devices. Proper ESD handling precautions need to be taken to avoid damage.

⚠ Do not cut any of the U1 socket pins until you have determined which pins are needed in your application. All of the PICOBEE I/O pins are the U1 socket pins. See [subsection 1.8](#) for pin removal information.

The Bill of Materials (BOM) and Component List are in [section 6](#). For full page assembly drawings see [Figure 1](#) (top) and [Figure 2](#) (bottom).

1.1 Bottom Side Components

- D1
Line the cathode marking on D1 with the cathode marking on the silkscreen
- D21, D22
Line the cathode marking of D21, D22 with the cathode marking on the silkscreen
- L1
The value of inductor L1 is not critical. Kits will contain an inductor with a value between 10 μ H and 20 μ H
- R1
10K Ω (brown, black, black, red, brown)

1.2 Real-time Clock Circuit Assembly

- X21 crystal
- U23 socket
- B21 battery holder
The battery holder consists of a holder and a negative contact. Solder the negative contact first.
-
- R22, R23
10K Ω (brown, black, black, red, brown)
- C23

1.3 XBee Circuit Assembly

- U24 (XBee sockets)
2 10x1 2mm center receptacles.
- C24
- D23, D24

1.4 Power Supply Circuit Assembly

Solder the top side components:

- C10, C11
*C10 and C11 are polarized parts. The long lead is the positive. The short lead is the negative. Make sure that the **positive** lead is inserted into positive hole in the PCB*
- U10
Make sure that the tab is aligned to the tab marking on the PCB.
- J10

1.5 Microcontroller Circuit Assembly

Solder the top side components:

- C1, C2, C3, C13, C4 (optional).
C4 is optional and is not included in the kit and is normally not required. It is meant for applications that require additional filtering of the reset line. The reset function that uses the /RTS line from the USB interface will not function with C4 installed.
- D2
The negative lead of the LED is the short lead. Align the short lead with the negative marking on the PCB.
- R2
374 Ω (orange, violet, yellow, black, brown).
- R3
10K Ω (brown, black, black, red, brown)
- J3
- J5
- X1, C5, C9
- U1 (socket)

1.6 Electro-mechanical Components

Since the reset switch (S1) is sensitive to washing it should be placed on last. Lightly clean the board after the switch is installed. If water does get into the switch let it dry out before applying power.

Solder the top side components:

- S1

1.7 IC Installation and Test

1.7.1 U23 (DS1337)

Remove the DS1337 from the antistatic foam and insert it into the socket aligning the notch in the IC package with the notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

PRELIMINARY

1.7.2 U1 (ATmega328P)

Remove the ATmega328P from the antistatic foam and insert it into the socket aligning the notch in the IC package with the notch mark indicated on the PCB silkscreen. Be careful to align pins on both sides of the socket prior to pressing the IC into the socket.

1.7.3 B21 (CR1220 coin cell)

Install a CR1220 coin cell into the battery holder (B21) observing the polarity indicated on the holder.

The PICOBEE should now be fully functional and is ready to program (see [section 5](#)). Depending on the application some of the pins on the U1 socket should be removed (see [subsection 1.8](#)).

1.8 Pin Removal

After operation of the PICOBEE is verified it is recommended that some of the U1 pins be cut flush to the PCB level. Each application is different and needs to be reviewed. Pins like XTAL1 and XTAL2 can be affected by stray capacitance and noise. For most applications cutting the XTAL1, XTAL2, AREF and AVCC is recommended.

If your application may change over time then leave all pins intact and use care in your layout.

1.8.1 XTAL Pins

The XTAL circuit is susceptible to stray capacitance and noise so pins 9 and 10 should be cut flush to the PCB.

1.8.2 AREF

If you are not using an external analog reference then cut pin 21 flush to the board.

1.8.3 AVCC

If you are not powering the ADC from a different source then pin 20 should be cut flush to the board.

2 IO Connectors

J5 USB header for an FTDI TTL-232R-3V3 cable.

J10 Input power jack. See [subsection 3.1](#)

3 Electrical Hints

3.1 Power Supply

The PICOBEE is powered by a DC output wall adapter with a 2,1mm barrel jack (the tip is positive). The output voltage of the adapter should be between 5.3V to 18V. The 5V connection on the FTDI connector is not used.

The input voltage is limited by the amount of power dissipated in the linear regulator (U4). This varies by application.

It is critical to keep the power dissipation in the LDO regulator (U4), to less than one watt. The voltage drop across U4 is

$$V_{drop} = V_{in} - V_{out}$$

Where V_{in} is the input voltage connected to J10 and V_{out} is the output voltage (see ??). The power dissipated in U4 is given by

$$P_{diss} = V_{drop} \cdot I_{system}$$

where I_{system} is the load of the PICOBEE plus its peripheral circuitry.

4 Real-Time Clock

The PICOBEE real-time clock (RTC) consists of a DS1337 that is powered by a CR1220 coin cell or the PICOBEE linear regulator (U10). The or'ing diodes, D21 and D22, will output the higher voltage to the RTC (U23).

Communication to the DS1337 is through the I²C interface (a.k.a. two-wire or TWI). The I²C pullup resistors are on board (10KΩ). The interrupt lines, /INTA and /INTB are jumpered to PC3 (Arduino pin 17) and PC0 (Arduino pin 14) respectively. There are no pullup resistors on the interrupt lines. If external pullups are not added then the internal pullups of the ATmega328P need to be used.

Programming the RTC requires a software library for the DS1337 and for the TWI interface. Both of these libraries are on the [wiblocks](#) site.

4.1 I²C Pullup Resistors

The maximum bus capacitance of the I²C bus is 400pF. Unless a large number of devices are on the bus or devices are connected using long cables PICOBEE system will not get close to this limit. The DS1337 represents a maximum load of 10pF.

The minimum pullup resistance is $966\Omega \left(\frac{V_{CC}-0.4V}{3mA}\right)$. The maximum value pullup resistance is

$$R_{pullup(max)} = \begin{cases} \frac{1000nS}{C_{BUS}} & \text{if } F_{SCL} \leq 100kHz, \\ \frac{300nS}{C_{BUS}} & \text{if } 100kHz < F_{SCL} \leq 400kHz. \end{cases}$$

where C_{BUS} is the maximum bus capacitance, , and V_{CC} is 3.3V for the PICOBEE.

With a 100pF load (10 times the DS1337 load), the maximum resistance for 400kHz operation is 3KΩ. For 100kHz the maximum resistance is 10KΩ. If only the DS1337 is on the I²C bus the maximum resistances would be 100KΩ

PRELIMINARY

(100kHz) and 30K Ω (400kHz). The minimum resistance, which is not dependent on bus capacitance, is 966 Ω for any operating frequency and C_{BUS} . (Atmel, 2009a)

CBUS Frequency	100pF		400pF	
	Resistance Min	Resistance Max	Resistance Min	Resistance Max
100kHz	1150 Ω	10K Ω	1150 Ω	2500 Ω
400kHz	1150 Ω	3K Ω	–Not Practical–	

Table 1: I²C Pullup Resistors

4.2 DS1337 Interrupt Lines

The DS1337 interrupt lines, /INTA and /INTB are jumpered to PC3 (Arduino pin 17) and PC0 (Arduino pin 14) respectively. To disconnect /INTA cut jumper J24. To disconnect /INTB cut jumper J27.

There are no pullup resistors connected to the interrupt lines. To use the interrupt lines with the ATmega328P the internal pull-up resistors need to be enabled. For the ATmega328P 20K Ω $\leq R_{pullup}$ \leq 50K Ω which is sufficient to pullup the DS1337 lines. (Atmel, 2009b).

4.3 RTC Battery Life

The DS1337 operates with a V_{CC} from 1.8V to 5.5V. When power is removed from the PICOBEE the DS1337 is in standby mode and the maximum standby current is 1.5 μ A (Maxim, 2009a). The CR1220 coin cell has a capacity of 40mAH (to 2V). The battery life is \approx 26000 hours.

4.4 Debug LED

The debug LED, D2, can be connected to U1 pin 13 (PD7) of the ATmega328P or left disconnected. U1 pin 13 corresponds to Arduino pin 7



LED jumper in the disconnected position



LED jumper in the PD7 position

4.5 Pinout

The input and output pins for the PICOBEE are the socket pins of the microcontroller (U1). The pinout is listed in Table 2.

Pin Number	Pin Name	Arduino Number	Notes
2	RXD	0	
3	TXD	1	
4	PD2	2	
5	PD3	3	
6	PD4	4	
11	PD5	5	
12	PD6	6	
13	PD7	7	Debug LED
14	PB0	8	
15	PB1	9	
16	PB2	10	
17	PB3	11	MOSI
18	PB4	12	MISO
19	PB5	13	SCK
23	PC0	A0	
24	PC1	A1	
25	PC2	A2	
26	PC3	A3	
27	PC4	A4	SDA
28	PC5	A5	SCL
1	Reset		
9	XTAL1		PB6
10	XTAL2		PB7
7	VCC		
20	AVCC		
21	AREF		
8	GND		
22	GND		

Table 2: U1 Pinout

5 Programming the PICOBEE

The PICOBEE can be programmed using the Arduino tools (version 0011 or later). Connect an FTDI TTL-232R-3V3 cable to header J5 with the black wire aligned to pin one.

5.1 Selecting the proper board

In order for the Arduino tools to recognize the wiblocks boards additional lines need to be added to the `boards.txt` file. The additional lines are shown in Listing 1 (with annotations). A file containing these additions can be downloaded from wiblocks.com. Once `boards.txt` is modified select `wiblocks 328 at 12MHz` from the `Tools->Board` menu.

5.2 Downloading a program

The PICOBEE must be rebooted to start the program download. This can be done by pressing the reset button S1 immediately before starting the download. If your USB port is configured to `set RTS on close` then the reset will occur automatically.

PRELIMINARY

Listing 1: boards.txt Modifications for the PICOBEE

```
1 wiblocks_328.name=wiblocks 328 at 12MHz
2 wiblocks_328.upload.protocol=stk500
3 wiblocks_328.upload.maximum_size=30720
4 wiblocks_328.upload.speed=19200
5 wiblocks_328.bootloader.low_fuses=0xff
6 wiblocks_328.bootloader.high_fuses=0xdd
7 wiblocks_328.bootloader.extended_fuses=0x00
8 wiblocks_328.bootloader.path=atmega328
9 wiblocks_328.bootloader.file=wiblocks_328.hex
10 wiblocks_328.bootloader.unlock_bits=0x3F
11 wiblocks_328.bootloader.lock_bits=0x0F
12 wiblocks_328.build.mcu=atmega328p
13 wiblocks_328.build.f_cpu=12000000L
14 wiblocks_328.build.core=arduino
```

PRELIMINARY

References

- Atmel. (2009a). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. , 323. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)
- Atmel. (2009b). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. , 314. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)
- Atmel. (2009c). 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash. (Retrieved March 14, 2009, from http://www.atmel.com/dyn/resources/prod_documents/doc8025.pdf)
- Maxim. (2009a, July). DS1337 I2C Serial Real-Time Clock. , 2-3. (Retrieved September 30, 2009, from <http://datasheets.maxim-ic.com/en/ds/DS1337-DS1337C.pdf>)
- Maxim. (2009b, July). DS1337 I2C Serial Real-Time Clock. (Retrieved September 30, 2009, from <http://datasheets.maxim-ic.com/en/ds/DS1337-DS1337C.pdf>)

PRELIMINARY

6 Assembly Documentation and Schematics

Table 3: Bill of Materials

Kit: PICOBEE-KIT

Qty	Reference	Part Number	Description
1	B21	CON_BAT_Keystone-500	connector, battery, CR1220
6	C1, C2, C3, C4, C13, C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
2	C5, C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
2	C10, C11	CAPPR_Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
1	C24	CAPR-1U00-10V-X5R-5MM	capacitor, ceramic, 1uF, 10%, 10V, X5R
1	D1	DIOA-1N4148	diode, 1N4148
3	D2, D23, D24	LEDR-1T-GRN-2M00	LED, T1, Green
2	D21, D22	DIOA-BAT41	diode, BAT41
1	J3	HDR_BR-3X1-100M	header, 3x1, 100mils
1	J5	HDR_BR-6X1-100M	header, 6x1, 100mils
1	J10	CON_CUI-PJ-202AH	power jack, 2.1mm
1	L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
4	R1, R3, R22, R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
3	R2, R25, R26	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
1	S1	SW_Panasonic_EVQ-PAE04M	pushbutton
1	S2	SW_CK_JS202011CQN	switch, CK JS202011CQN
1	U1	IC_ATMEL_ATmega168-20PU	ATmega168-20PU
1	U10	VREG_On-Semi_MC33269T-3.3G	voltage regulator, 3.3V, 800mA, TO-220
1	U23	IC_RTC_Maxim_DS1337+	IC, RTC, DS1337+
1	X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
1	X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
1		DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
1		JMP_Adamtech_MSBHG	Shunt with handle
1		DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
1		CON_BAT_Keystone_2990	connector, battery, negative-contact, CR1220
2		HDRF-10x1-2MM	header, recptacle, 10x1, 2mm
1		wiblock_PICOBEE-PCB	

PRELIMINARY

Table 4: Component List

Kit: PICOBEE-KIT

Reference	Part Number	Description
B21	CON_BAT_Keystone_500	connector, battery, CR1220
C1	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C2	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C3	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C4	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C13	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C23	CAPR-0U10-50V-X7R-100M	capacitor, ceramic, 0.1uF, 10%, 50V, X7R
C5	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C9	CAPR-20P0-100V-NPO-5T00	capacitor, ceramic, 20pF
C10	CAPPR_Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
C11	CAPPR_Nichicon_UPW1E100MDD	capacitor, Nichicon UPW1E100MDD
C24	CAPR-1U00-10V-X5R-5MM	capacitor, ceramic, 1uF, 10%, 10V, X5R
D1	DIOA-1N4148	diode, 1N4148
D2	LEDR-1T-GRN-2M00	LED, T1, Green
D23	LEDR-1T-GRN-2M00	LED, T1, Green
D24	LEDR-1T-GRN-2M00	LED, T1, Green
D21	DIOA-BAT41	diode, BAT41
D22	DIOA-BAT41	diode, BAT41
J3	HDR_BR-3X1-100M	header, 3x1, 100mils
J5	HDR_BR-6X1-100M	header, 6x1, 100mils
J10	CON_CUI-PJ-202AH	power jack, 2.1mm
L1	INDA-10UH-130M-10T0	inductor, 10uH, 10%
R1	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R3	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R22	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R23	RES-10K0-0W125-1T00	resistor, 10K, 1/8W, 1%
R2	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
R25	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
R26	RES-374R-0W125-1T00	resistor, 374 Ohm, 1/8W, 1%
S1	SW_Panasonic_EVQ-PAE04M	pushbutton
S2	SW_CK_JS202011CQN	switch, CK JS202011CQN
U1	IC_ATMEL_ATmega168-20PU	ATmega168-20PU
U10	VREG_On-Semi_MC33269T-3.3G	voltage regulator, 3.3V, 800mA, TO-220
U23	IC_RTC_Maxim_DS1337+	IC, RTC, DS1337+
X1	XTAL-12M-20P-HC49US	crystal, 12MHz, 20pF, HC49US
X21	XTAL-32K768-6P-2X6	crystal, 32.768KHz, 6pF, 2x6mm package
	DIP-8P-300M	DIP Socket, 8 Pin, 300mil centers
	JMP_Adamtech_MSBHG	Shunt with handle
	DIP_WW-28P-300M	DIP Socket, 28 Pin, 300mil centers, Wire Wrap
	CON_BAT_Keystone_2990	connector, battery, negative-contact, CR1220
	HDRF-10x1-2MM	header, recptacle, 10x1, 2mm
	wiblock_PICOBEE-PCB	

PRELIMINARY

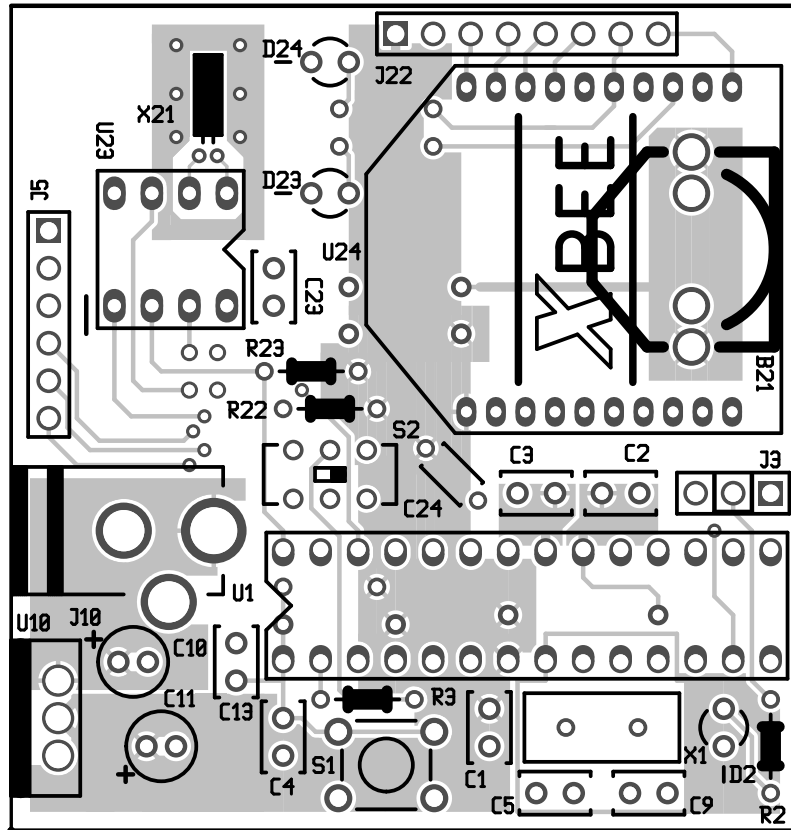


Figure 1: PICOBEE Top Side Assembly Drawing (Rev 0)

PRELIMINARY

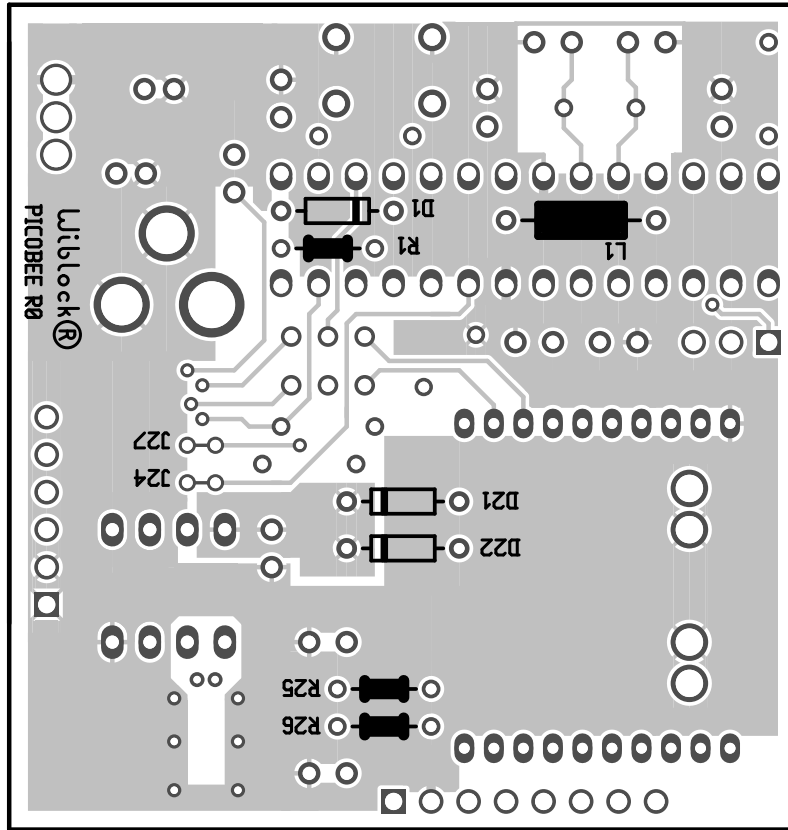
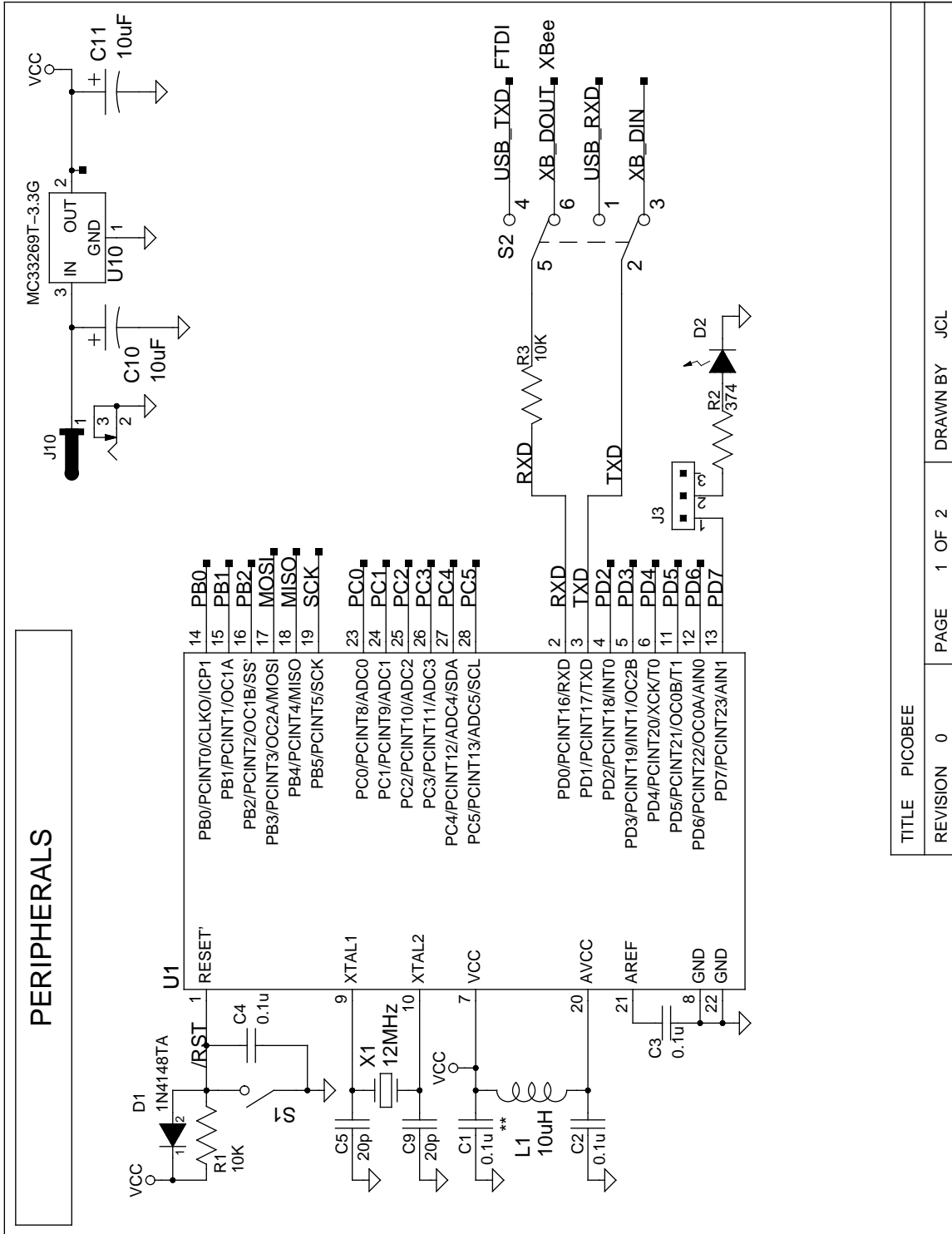


Figure 2: PICOBEE Bottom Side Assembly Drawing (Rev 0)



TITLE	PICOBEE
REVISION	0
PAGE	1 OF 2
DRAWN BY	JCL

Figure 3: PICOBEE (Rev 0)

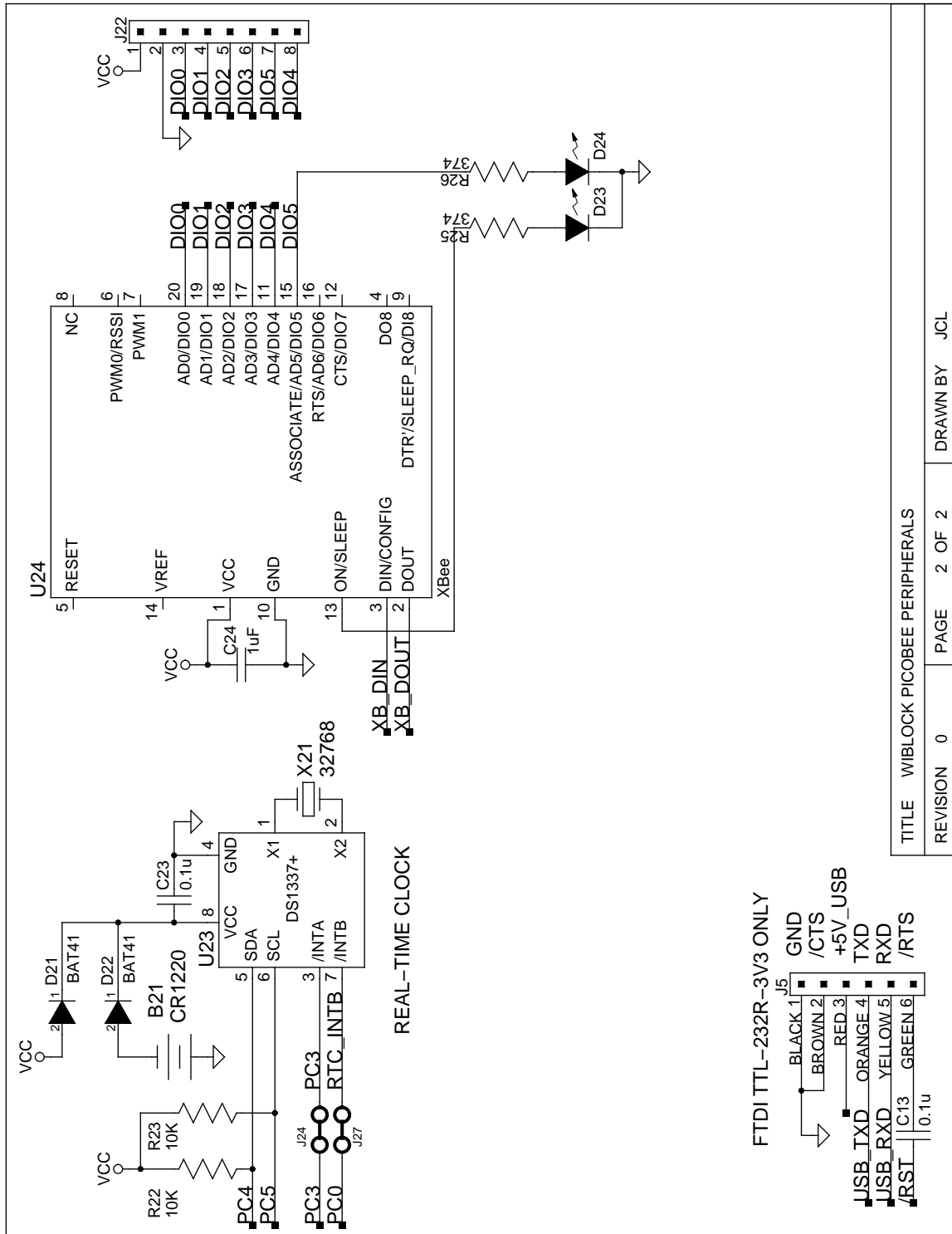


Figure 4: PICOBEE (Rev 0)

PRELIMINARY

19-4652; 7/09



DS1337 I²C Serial Real-Time Clock

www.maxim-ic.com

GENERAL DESCRIPTION

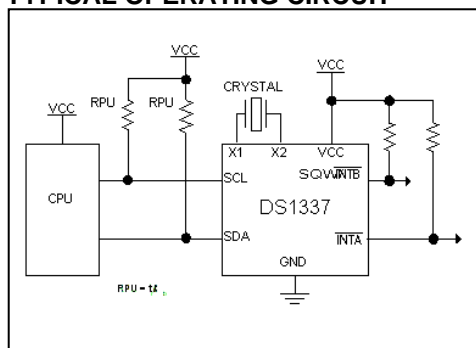
The DS1337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I²C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The device is fully accessible through the serial interface while V_{CC} is between 1.8V and 5.5V. I²C operation is not guaranteed below 1.8V. Timekeeping operation is maintained with V_{CC} as low as 1.3V.

APPLICATIONS

Handhelds (GPS, POS Terminal, MP3 Player)
Consumer Electronics (Set-Top Box, VCR/Digital Recording)
Office Equipment (Fax/Printer, Copier)
Medical (Glucometer, Medicine Dispenser)
Telecommunications (Router, Switch, Server)
Other (Utility Meter, Vending Machine, Thermostat, Modem)

TYPICAL OPERATING CIRCUIT



Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata.

FEATURES

- Real-Time Clock (RTC) Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Valid Up to 2100
- Available in a Surface-Mount Package with an Integrated Crystal (DS1337C)
- I²C Serial Interface
- Two Time-of-Day Alarms
- Oscillator Stop Flag
- Programmable Square-Wave Output Defaults to 32kHz on Power-Up
- Available in 8-Pin DIP, SO, or μ SOP
- 40°C to +85°C Operating Temperature Range

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1337+	-40°C to +85°C	8 DIP (300 mils)	DS1337
DS1337S+	-40°C to +85°C	8 SO (150 mils)	DS1337
DS1337U+	-40°C to +85°C	8 μ SOP	1337
DS1337C#	-40°C to +85°C	16 SO (300 mils)	DS1337C

+ Denotes a lead(Pb)-free/RoHS-compliant device.
Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements. The lead finish is JEDEC category e3, and is compatible with both lead-based and lead-free soldering processes.
† A "+" anywhere on the top mark denotes a lead-free device. A "#" denotes a RoHS-compliant device.

Pin Configurations appear at end of data sheet.

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.3V to +6.0V
 Operating Temperature Range (Noncondensing).....-40°C to +85°C
 Storage Temperature Range.....-55°C to +125°C
 Soldering Temperature.....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CC} Supply Voltage	V _{CC}	Full operation	1.8	3.3	5.5	V
	V _{CC(T)}	Timekeeping (Note 5)	1.3		1.8	V
Logic 1	V _{IH}	SCL, SDA	0.7 x V _{CC}		V _{CC} + 0.3	V
		$\overline{\text{INTA}}$, SQW/ $\overline{\text{INTB}}$			5.5	
Logic 0	V _{IL}		-0.3	+0.3 x V _{CC}		V

DC ELECTRICAL CHARACTERISTICS—Full Operation

(V_{CC} = 1.8V to 5.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I _{LI}	(Note 2)	-1		+1	μA
I/O Leakage	I _{LO}	(Note 3)	-1		+1	μA
Logic 0 Output (V _{OL} = 0.4V)	I _{OL}	(Note 3)			3	mA
Active Supply Current	I _{CCA}	(Note 4)			150	μA
Standby Current	I _{CCS}	(Notes 5, 6)			1.5	μA

DC ELECTRICAL CHARACTERISTICS--Timekeeping

(V_{CC} = 1.3V to 1.8V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timekeeping Current (Oscillator Enabled)	I _{CC(T)OSC}	(Notes 5, 7, 8, 9)		425	600	nA
Data-Retention Current (Oscillator Disabled)	I _{CC(T)DDR}	(Notes 5, 9)			100	nA

PRELIMINARY

DS1337 I²C Serial Real-Time Clock

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.8V to 5.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f _{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between a STOP and START Condition	t _{BUF}	Fast mode	1.3			μs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 10)	t _{HD:STA}	Fast mode	0.6			μs
		Standard mode	4.0			
LOW Period of SCL Clock	t _{LOW}	Fast mode	1.3			μs
		Standard mode	4.7			
HIGH Period of SCL Clock	t _{HIGH}	Fast mode	0.6			μs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	t _{SU:STA}	Fast mode	0.6			μs
		Standard mode	4.7			
Data Hold Time (Notes 11, 12)	t _{HD:DAT}	Fast mode	0		0.9	μs
		Standard mode	0			
Data Setup Time (Note 13)	t _{SU:DAT}	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 14)	t _R	Fast mode	20 + 0.1C _B		300	ns
		Standard mode	20 + 0.1C _B		1000	
Fall Time of Both SDA and SCL Signals (Note 14)	t _F	Fast mode	20 + 0.1C _B		300	ns
		Standard mode	20 + 0.1C _B		300	
Setup Time for STOP Condition	t _{SU:STO}	Fast mode	0.6			μs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C _B	(Note 14)			400	pF
I/O Capacitance (SDA, SCL)	C _{I/O}	(Note 15)			10	pF
Oscillator Stop Flag (OSF) Delay	t _{OSF}			100		ms

Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: SCL only.

Note 3: SDA, $\overline{\text{INTA}}$, and $\overline{\text{SQW/INTB}}$.

Note 4: I_{CCA}—SCL clocking at max frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 5: Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}.

Note 6: SQW enabled.

Note 7: Specified with the SQW function disabled by setting INTCN = 1.

Note 8: Using recommended crystal on X1 and X2.

Note 9: The device is fully accessible when 1.8 ≤ V_{CC} ≤ 5.5V. Time and date are maintained when 1.3V ≤ V_{CC} ≤ 1.8V.

Note 10: After this period, the first clock pulse is generated

Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 12: The maximum t_{HD:DAT} need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 13: A fast-mode device can be used in a standard-mode system, but the requirement t_{SU:DAT} ≥ 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{Rmax} + t_{SU:DAT} = 1000 + 250 = 1250ns before the SCL line is released.

Note 14: C_B—total capacitance of one bus line in pF.

Note 15: Guaranteed by design. Not production tested.

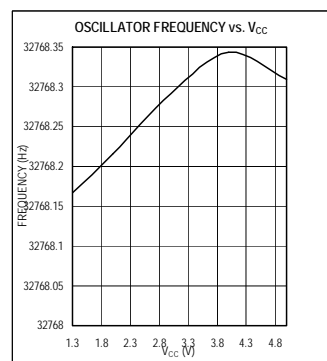
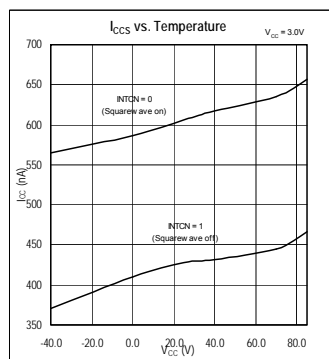
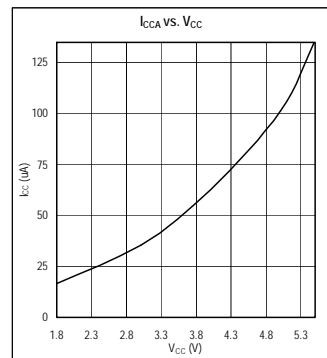
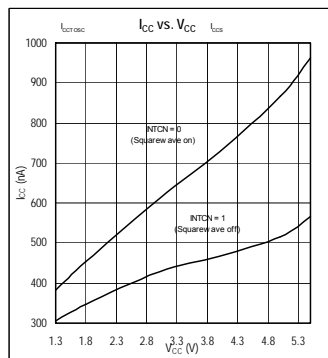
PRELIMINARY

DS1337 I²C Serial Real-Time Clock

Note 16: The parameter t_{OSF} is the period of time that the oscillator must be stopped for the OSF bit to be set over the voltage range of $V_{CC(MIN)} \leq V_{CC} \leq V_{CC(MAX)}$.

TYPICAL OPERATING CHARACTERISTICS

($V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

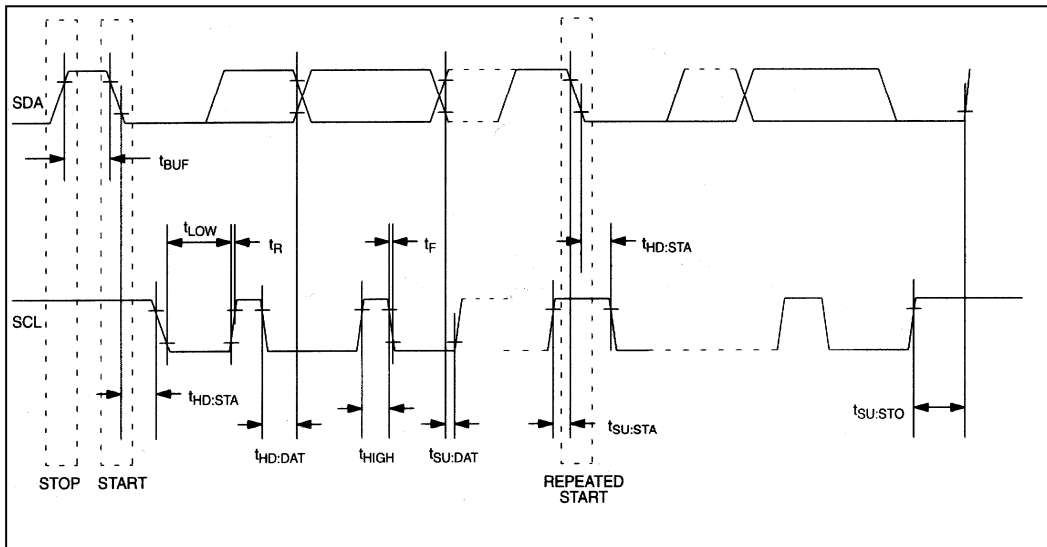


PRELIMINARY

PIN DESCRIPTION

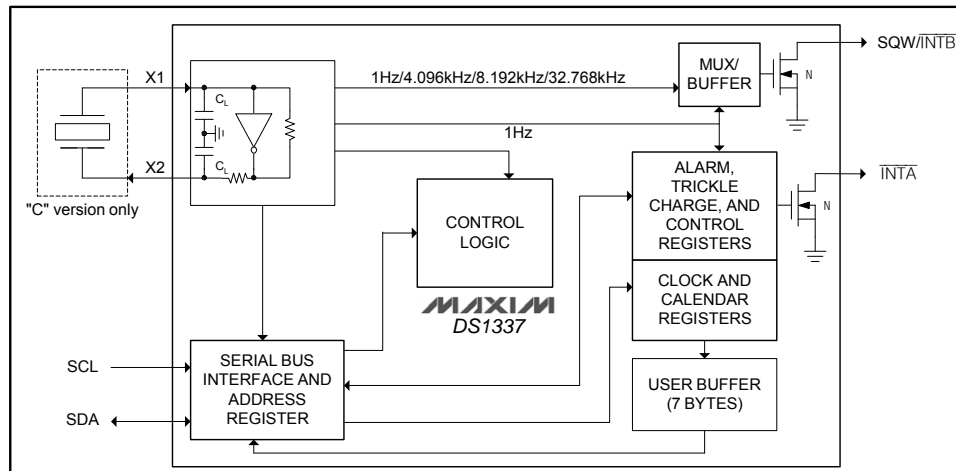
PIN		NAME	FUNCTION
8	16		
1	—	X1	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. For more information about crystal selection and crystal layout considerations, refer to <i>Application Note 58: Crystal Considerations with Dallas Real-Time Clocks</i> . An external 32.768kHz oscillator can also drive the DS1337. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
2	—	X2	
3	14	$\overline{\text{INTA}}$	Interrupt Output. When enabled, $\overline{\text{INTA}}$ is asserted low when the time/day/date matches the values set in the alarm registers. This pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC} . If not used, this pin may be left floating.
4	15	GND	Ground. DC power is provided to the device on this pin.
5	16	SDA	Serial Data Input/Output. SDA is the input/output pin for the I ² C serial interface. The SDA pin is open-drain output and requires an external pullup resistor.
6	1	SCL	Serial Clock Input. SCL is used to synchronize data movement on the serial interface.
7	2	SQW/ $\overline{\text{INTB}}$	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V, regardless of the voltage on V_{CC} . If not used, this pin may be left floating.
8	3	V_{CC}	DC Power. DC power is provided to the device on this pin.
—	4–13	N.C.	No Connect. These pins are not connected internally, but must be grounded for proper operation.

TIMING DIAGRAM



PRELIMINARY

BLOCK DIAGRAM



DETAILED DESCRIPTION

The *Block Diagram* shows the main elements of the DS1337. As shown, communications to and from the DS1337 occur serially over an I²C bus. The DS1337 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible through the I²C interface whenever V_{CC} is between 5.5V and 1.8V. I²C operation is not guaranteed when V_{CC} is below 1.8V. The DS1337 maintains the time and date when V_{CC} is as low as 1.3V.

OSCILLATOR CIRCUIT

The DS1337 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. [Table 1](#) specifies several crystal parameters for the external crystal. The *Block Diagram* shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f ₀		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C _L		6		pF

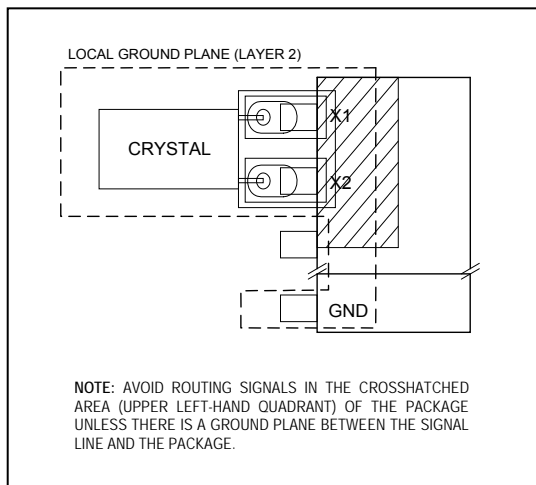
*The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.

PRELIMINARY

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. [Figure 1](#) shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Figure 1. Typical PC Board Layout for Crystal



DS1337C ONLY

The DS1337C integrates a standard 32,768Hz crystal in the package. Typical accuracy at nominal V_{CC} and +25°C is approximately +10ppm. Refer to *Application Note 58* for information about crystal accuracy vs. temperature.

OPERATING MODES

The amount of current consumed by the DS1337 is determined, in part, by the I²C interface and oscillator operation. The following table shows the relationship between the operating mode and the corresponding I_{CC} parameter.

Operating Mode	V_{CC}	Power
I ² C Interface Active	$1.8V \leq V_{CC} \leq 5.5V$	I_{CC} Active (I_{CCA})
I ² C Interface Inactive	$1.8V \leq V_{CC} \leq 5.5V$	I_{CC} Standby (I_{CCS})
I ² C Interface Inactive	$1.3V \leq V_{CC} \leq 1.8V$	Timekeeping (I_{CCTOSC})
I ² C Interface Inactive Oscillator Disabled	$1.3V \leq V_{CC} \leq 1.8V$	Data Retention (I_{CCTDDR})

PRELIMINARY

ADDRESS MAP

Table 2 shows the address map for the DS1337 registers. During a multibyte access, when the address pointer reaches the end of the register space (0Fh) it wraps around to location 00h. On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 2. Timekeeper Registers

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds			Seconds	Seconds	00–59
01H	0	10 Minutes			Minutes			Minutes	Minutes	00–59
02H	0	12/24	AM/PM	10 Hour	Hour			Hours	1–12 + AM/PM	00–23
			10 Hour							
03H	0	0	0	0	0	Day		Day	1–7	
04H	0	0	10 Date		Date			Date	Date	01–31
05H	Century	0	0	10 Month	Month			Month/ Century	01–12 + Century	
06H	10 Year				Year			Year	Year	00–99
07H	A1M1	10 Seconds			Seconds			Alarm 1 Seconds	Alarm 1 Seconds	00–59
08H	A1M2	10 Minutes			Minutes			Alarm 1 Minutes	Alarm 1 Minutes	00–59
09H	A1M3	12/24	AM/PM	10 Hour	Hour			Alarm 1 Hours	1–12 + AM/PM	00–23
			10 Hour							
0AH	A1M4	DY/DT	10 Date		Day			Alarm 1 Day	1–7	
					Date			Alarm 1 Date	01–31	
0BH	A2M2	10 Minutes			Minutes			Alarm 2 Minutes	Alarm 2 Minutes	00–59
0CH	A2M3	12/24	AM/PM	10 Hour	Hour			Alarm 2 Hours	1–12 + AM/PM	00–23
			10 Hour							
0DH	A2M4	DY/DT	10 Date		Day			Alarm 2 Day	1–7	
					Date			Alarm 2 Date	01–31	
0EH	$\overline{E}OSC$	0	0	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	—

Note: Unless otherwise specified, the state of the registers is not defined when power is first applied or V_{CC} falls below the V_{OSC} .

I²C INTERFACE

The I²C interface is accessible whenever V_{CC} is at a valid level. If a microcontroller connected to the DS1337 resets while reading from the DS1337 during an I²C read, the two could become unsynchronized. The microcontroller must terminate the last byte read with a Not-Acknowledge (NACK) to properly terminate the read. When the microcontroller resets, the DS1337 I²C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

PRELIMINARY

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in [Table 2](#). The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enable, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The DS1337 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{\text{AM/PM}}$ bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). All hours values, including the alarms, must be reinitialized whenever the 12/24-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99–00.

ALARMS

The DS1337 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h–0Ah. Alarm 2 can be set by writing to registers 0Bh–0Dh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes—each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits ([Table 2](#)). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. [Table 3](#) shows the possible settings. Configurations not listed in the table result in illogical operation.

The $\overline{\text{DY/DT}}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If $\overline{\text{DY/DT}}$ is written to logic 0, the alarm is the result of a match with date of the month. If $\overline{\text{DY/DT}}$ is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. The bit(s) will remain at a logic 1 until written to a logic 0 by the user. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{\text{INTA}}$ or $\overline{\text{SQW/INTB}}$) signals. The match is tested on the once-per-second update of the time and date registers.

PRELIMINARY

Table 3. Alarm Mask Bits

DY/ \overline{DT}	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/ \overline{DT}	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL-PURPOSE REGISTERS

The DS1337 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\overline{EOSC}	0	0	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator (\overline{EOSC}). This active-low bit when set to logic 0 starts the oscillator. When this bit is set to logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

SQW/ \overline{INTB} Output

INTCN	RS2	RS1	SQW/ \overline{INTB} OUTPUT	A2IE
0	0	0	1Hz	X
0	0	1	4.096kHz	X
0	1	0	8.192kHz	X
0	1	1	32.768kHz	X
1	X	X	$\overline{A2F}$	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers activates the \overline{INTA} pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/ \overline{INTB} pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/ \overline{INTB} pin. This bit is set to logic 0 when power is first applied.

PRELIMINARY

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{\text{INTA}}$ (when $\text{INTCN} = 0$) or to assert $\text{SQW}/\overline{\text{INTB}}$ (when $\text{INTCN} = 1$). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{\text{INTA}}$. When the A1IE bit is set to logic 0, the A1F bit does not initiate the $\overline{\text{INTA}}$ signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

- 1) The first time power is applied.
- 2) The voltage present on V_{CC} is insufficient to support oscillation.
- 3) The $\overline{\text{EOSC}}$ bit is turned off.
- 4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on either $\overline{\text{INTA}}$ or $\text{SQW}/\overline{\text{INTB}}$ depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the $\overline{\text{INTA}}$ pin goes low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the $\text{SQW}/\overline{\text{INTB}}$ pin goes low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{\text{INTA}}$ pin goes low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

PRELIMINARY

I²C SERIAL DATA BUS

The DS1337 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1337 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS1337 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined ([Figure 2](#)):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

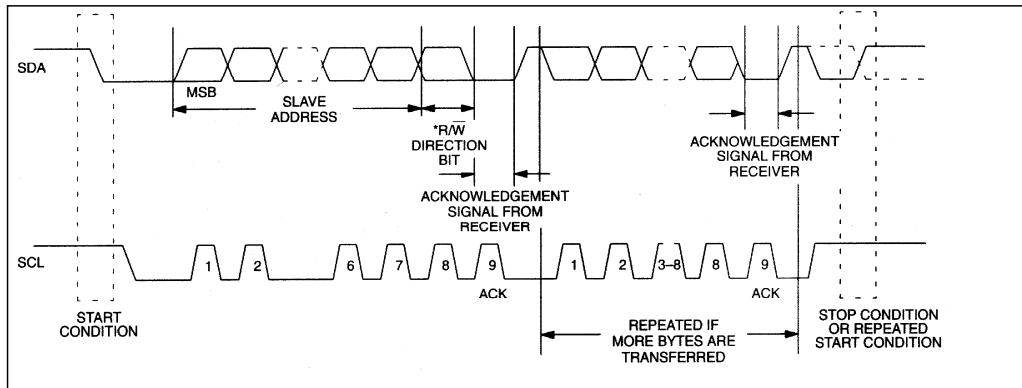
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

PRELIMINARY

Figure 2. Data Transfer on I²C Serial Bus



Depending upon the state of the $\overline{R/W}$ bit, two types of data transfer are possible:

- 1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
- 2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1337 can operate in the following two modes:

- 1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 3). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit ($\overline{R/W}$), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the DS1337 acknowledges the slave address + write bit, the master transmits a register address to the DS1337. This sets the register pointer on the DS1337. The master may then transmit zero or more bytes of data, with the DS1337 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.
- 2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1337 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 4 and Figure 5). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS1337 address, which is 1101000, followed by the direction bit ($\overline{R/W}$), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The DS1337 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1337 must receive a "not acknowledge" to end a read.

PRELIMINARY

Figure 3. Data Write—Slave Receiver Mode

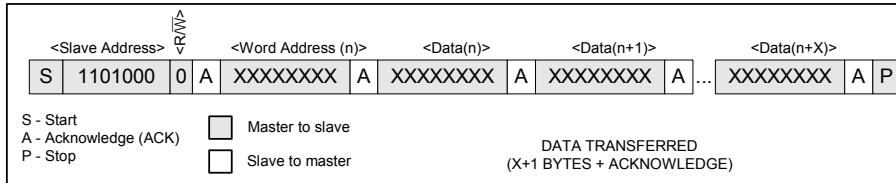


Figure 4. Data Read (from Current Pointer Location)—Slave Transmitter Mode

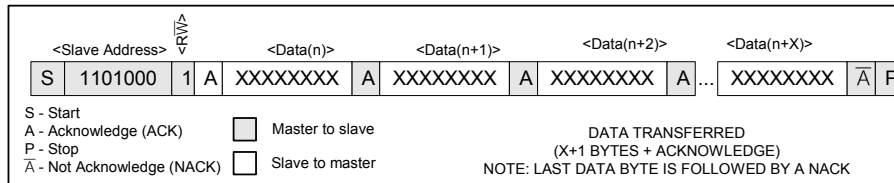
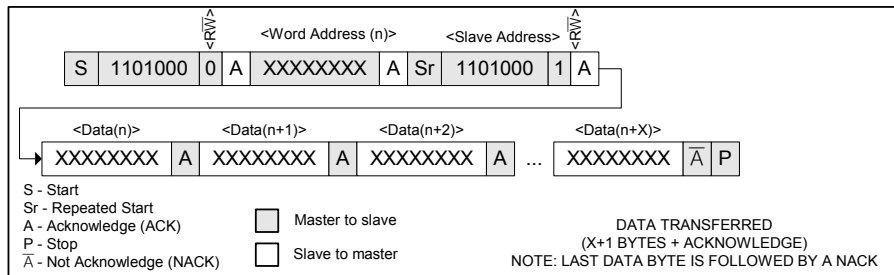


Figure 5. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



PRELIMINARY

DS1337 I²C Serial Real-Time Clock

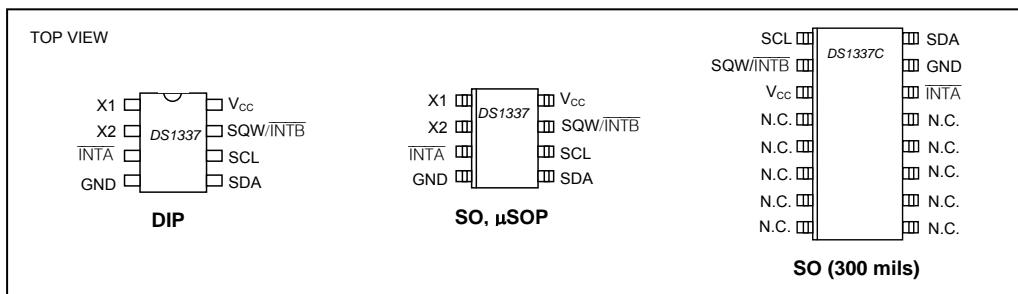
HANDLING, PC BOARD LAYOUT, AND ASSEMBLY

The DS1337C package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

PIN CONFIGURATIONS



CHIP INFORMATION

TRANSISTOR COUNT: 10,950
PROCESS: CMOS

THERMAL INFORMATION

PACKAGE	THETA-J _A (°C/W)	THETA-J _C (°C/W)
8 DIP	110	40
8 SO	170	40
8 μ SOP	229	39
16 SO	73	23

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 PDIP	P8+8	21-0043
8 SO	S8+2	21-0041
8 μ MAX	U8+1	21-0036
16 SO	W16-H2	21-0042

PRELIMINARY

DS1337 I²C Serial Real-Time Clock

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
080508	Added device access details to <i>General Description</i> section.	1
	Removed leaded ordering numbers from the <i>Ordering Information</i> table.	1
	Added Note 5 to Timekeeping V_{CC} EC table range.	2
	Added "Full Operation" and "Timekeeping" to headers to clarify table usage.	2
	Added OSF parameter to EC table.	3
	Updated <i>Pin Description</i> to indicate max input voltage and that unused outputs may be left open.	5
	Added oscillator circuit and show open-drain transistors on <i>Block Diagram</i> .	6
	Added <i>Operating Mode</i> section with details on operating mode and corresponding I_{CC} parameter.	7
	Added <i>I²C Interface</i> section explaining how to synchronize a microcontroller and the RTC.	8
071609	Corrected legend in figure 5 for not-acknowledge (add overbar to symbol).	14
	Removed conflicting SDA/SCL input bias statement in <i>Pin Description</i> .	5

16 of 16

Maxim/Dallas Semiconductor cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim/Dallas Semiconductor product. No circuit patent licenses are implied. Maxim/Dallas Semiconductor reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

© 2009 Maxim Integrated Products

The Maxim logo is a registered trademark of Maxim Integrated Products, Inc. The Dallas logo is a registered trademark of Dallas Semiconductor.